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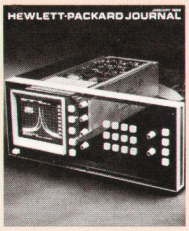

Electronic instruments and systems usually have a display of some kind to present data to humans in a readily understandable form. More and more, such systems have microcomputers inside, and while they may be fed continuously varying real-world quantities like voltages, speeds, and temperatures, the first thing they do with this analog data is convert it to binary numbers so that internally they can operate entirely digitally. This month's cover subject, the 1345A Graphics Display Module, is a high-quality cathode ray tube display that's designed to be built into spectrum analyzers, network analyzers, and other electronic instruments based on microcomputers. The 1345A is easy for a microcomputer to talk to, because it understands picture descriptions in a simple binary language. With it, an instrument designer can provide high-quality graphics and text while avoiding the time and expense required to design a custom display. Among the 1345A's contributions are its speed, line quality, resolution, number of brightness levels, and compactness—the entire module is only a little larger than the CRT. It tests itself, too. The design story begins on page 20.

Complex digital systems, especially computers and microcomputer-based products, are particularly difficult to troubleshoot. If you connect an oscilloscope to any point in a digital circuit, you see a voltage switching rapidly between two levels. Without specialized test equipment and detailed knowledge of the system, it isn't possible to tell whether that "bit stream," as it's called, is correct. Yet it's impractical for every field service technician to have that kind of knowledge and equipment. Signature analysis was developed as a response to this problem. Guided by a test procedure, the technician probes points in the system and observes four letters and/or numbers (a signature) displayed by a compact instrument (a signature analyzer). Comparing these signatures with documented correct signatures tells at once whether things are as they should be. The catch is that the system has to be designed for this kind of troubleshooting so that when it's being tested, known bit streams can be introduced and the system can be set up so that signatures throughout it are predictable. But what about all the products that were designed without this capability? Can't they be retrofit for signature analysis? Yes, they can, but it's not easy; some redesign is usually necessary. Again a problem, and again a solution, the 5001A/B/C/D Microprocessor Exercisers. The four versions of this instrument make it easy to retrofit products based on four widely used microprocessors without costly redesign. How does it work? The story begins on page 9.

Last month's issue reported on HP developments in surface acoustic waves, or SAWs, and described SAW delay lines, filters, resonators, and sensors. In this issue, on page 3, you can read how SAWs can be used to do exotic signal processing, such as pulse compression, variable-bandwidth filtering, matched filtering, variable time delay, adaptive filtering, correlation, convolution, and Fourier transformation. Compared to digital processors that do the same things, SAW devices are small, simple, and rugged, operate in real time, and don't require high-accuracy analog-to-digital conversion. Their disadvantage is a limited dynamic range.

This month we're doing something we haven't done in our 32-year history. We're asking you, our readers, to tell us what you think of this publication. In the center of this issue we've put a reader opinion questionnaire. Please help us by completing it and mailing it back to us. If someone's already removed the questionnaire, your comments are welcome without it, now or at any time.

-R. P. Dolan

Signal Processing Using Surface Acoustic Waves

If electrical signals are converted into minute acoustic waves on the surface of a piezoelectric crystal, the signals can be processed in novel ways for various electronic applications. Such devices are small, rugged, and can be fabricated using microelectronic techniques.

by William R. Shreve

SURFACE-ACOUSTIC-WAVE (SAW) devices can be used for analog signal processing other than basic filtering and frequency control.[1] By tailoring the characteristics of a device to a particular application's requirement, one can design systems to do pulse compression, variable-bandwidth filtering, matched filtering, variable time delay, adaptive filtering, correlation, convolution or Fourier transformation. The major advantages of SAW components are real-time processing, small size and simplicity. The disadvantage is a limited dynamic range. Digital systems performing the same operations are capable of greater flexibility and accuracy at the expense of increased processing time and the high precision of analog-to-digital (A-to-D) conversion required at the input.

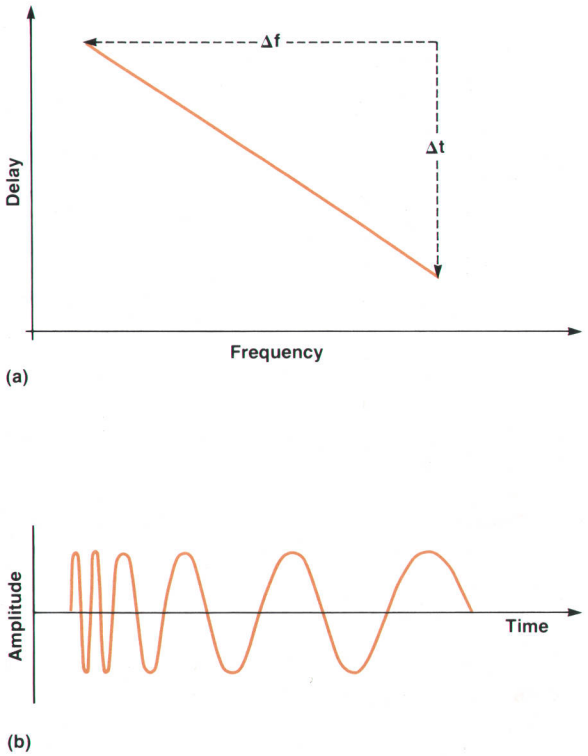

Fig. 1. *(a) Delay characteristic of linearly dispersive (down-chirp) filter. (b) Impulse response of same filter.*

Dispersive Delay Lines

A number of signal processing functions can be performed with dispersive delay lines. A dispersive delay line is a filter whose delay is a function of the input frequency. Fig. 1 shows the characteristics of a linearly dispersive delay line or chirp filter. The different frequency components of a short-duration, broadband input pulse are spread out in time as they pass through the filter. This spreading causes a reduction in peak power. Conversely, an appropriately matched chirp (spread-frequency) input signal is compressed in time by the filter. This compression improves the signal-to-noise ratio and simultaneously reduces the duration of the signal.

The first application of these devices was pulse compression for radar systems like that shown in Fig. 2.[2] An initial pulse is expanded in time, usually in a filter with a linear dispersion characteristic, amplified, and transmitted with all frequency components at the same power level to maximize the transmitted power. The received signal is compressed in another dispersive filter to enhance the signal-to-noise ratio. This system makes efficient use of transmitter power, increases the system's resolving capability in both range and velocity and reduces interference from other signals.

Chirp filters have also been used for variable-bandpass filters.[3] A pulse compressor and expander like those used in the radar system can be combined with a mixer as shown in Fig. 3. The passband of the system is determined by the overlap of the passbands of the two chirp filters and the relative offset is determined by the mixing frequency f_c.

Chirp filters can also be used to perform analog Fourier transform operations.[4] As shown in Fig. 4, the input signal is mixed with a chirp signal, passed through a matched chirp filter and postmultiplied by another chirp signal. Mathematically this can be expressed as follows:

$$F(t) = \{[S(t)\cdot C_1(t)] * C_3(t)\}\cdot C_2(t) \qquad (1)$$

If S(t) is a bandlimited signal and $C_1(t)$ and $C_2(t)$ are identical constant-amplitude chirp signals matched to the uniform filter impulse response $C_3(t)$, then F(t) becomes

$$F(t) = \exp(j4\pi f_1 t)\int_{-\Delta t/2}^{\Delta t/2} S(t)\exp(-j2\pi f\tau)\,d\tau \qquad (2)$$

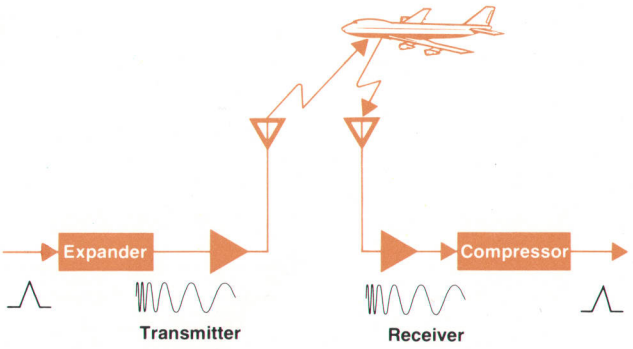

Fig. 2. *SAW devices can be used in chirp radar systems by expanding a pulse before it is transmitted and compressing the received signal back into a narrow pulse so that distance accuracy is maintained. Expanding a pulse reduces the peak transmitter power required and pulse compression improves the signal-to-noise ratio in the receiver.*

where $f = (\Delta f/\Delta t)t$, Δt is the length of the mixing chirp signal $C_1(t)$, and f_1 is the center frequency of that signal. This expression is the Fourier transform of the signal S(t) over the time interval Δt. For signals longer than Δt, the filter output from one Δt interval will interfere with the output from the next interval. Therefore, two channels would be required in parallel with appropriate switching for continuous transformation. The signal bandwidth must be limited to the difference between the filter bandwidth and the mixing chirp signal bandwidth. The circuit shown in Fig. 4 is significant because it can be used as a real-time equivalent of the digital Fourier transform to do spectrum analysis, convolution, or correlation. SAW devices can be used for the chirp filter and to generate the mixing chirp signals. Signal processing system capabilities depend on filters with large dispersion time and large bandwidth because these two parameters determine the maximum data rate and dynamic range of a system.

The accessibility of surface waves and their nondispersive propagation characteristics make chirp-filter design straightforward. Controlled variation of delay as a function of frequency is accomplished by choosing the appropriate transducer electrode pattern.

In SAW devices, the delay is proportional to the length of the propagation path, which in turn is determined by the distance between the input and output transducers. The frequency of the wave launched by a transducer is determined by the electrode spacing. Hence, frequency and

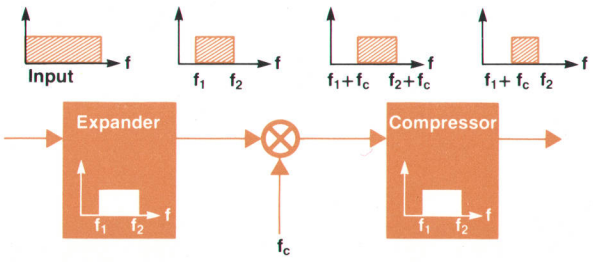

Fig. 3. *SAW chirp filters can be used for variable bandwidth filters as shown in the simple block diagram above. As the mixing frequency f_c increases the output bandwidth narrows.*

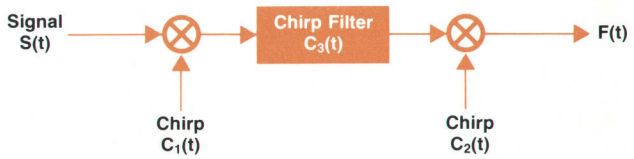

Fig. 4. *Chirp filter implementation of analog Fourier transform. Chirps $C_1(t)$ and $C_2(t)$ can be generated by pulsing SAW chirp filters. The output F(t) is the Fourier transform of the signal S(t).*

delay can be changed and controlled by the size and spacing of the transducers. Three transducer designs (Fig. 5) have been used for dispersive delay lines.[5] One uses a single, long dispersive transducer with a short, nondispersive, broadband transducer as the other port (Fig. 5a). This technique requires weighting* of only one transducer and is therefore the most straightforward and most easily analyzed. It has the disadvantage that it is difficult to match the nondispersive transducer over a broad frequency range

*Here weighting is the variation of the lengths of the electrode fingers in a transducer to achieve a desired impulse response.

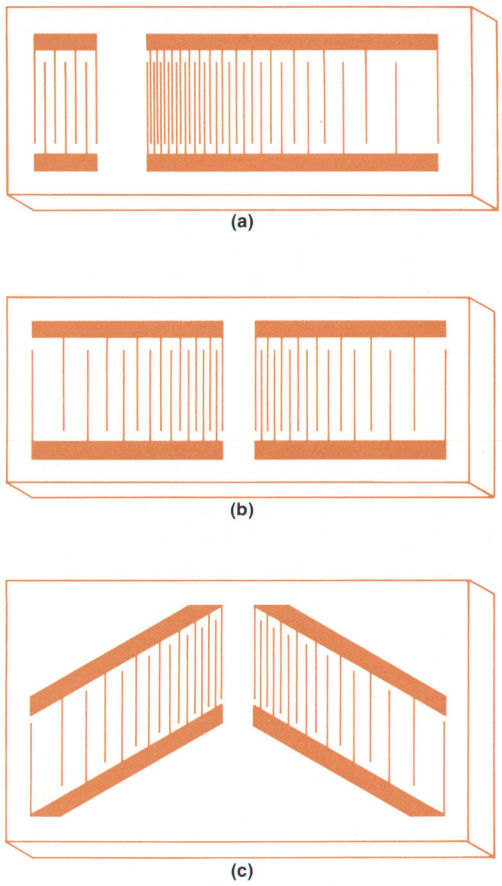

Fig. 5. *Three SAW transducer configurations used to make dispersive (chirp) filters. (a) Broadband, nondispersive transducer on the right, dispersive transducer on the left. (b) Both transducers are dispersive and shorter than the long one in (a). (c) Slanted arrangement of transducers used in (b). This minimizes distortion caused by propagation under transducer electrodes.*

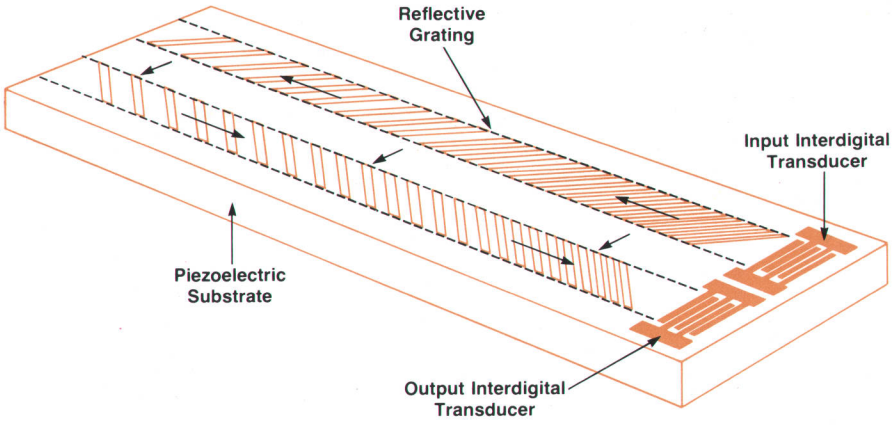

Fig. 6. *Reflective array compressor. Here two broadband transducers are used for the input and output and dispersion is obtained from the variation in path length for different frequencies. The wave is reflected when the spacing in the direction of propagation is a wavelength λ (the period for adjacent grooves in the grating is about $\lambda/\sqrt{2}$).*

and still achieve low insertion loss.

In the configuration of Fig. 5b, two transducers are used to achieve the dispersive characteristic. Each transducer contains fewer fingers than the one dispersive transducer in the configuration of Fig. 5a and is therefore easier to match. A broadband nondispersive transducer is not required. The resulting filter will have lower loss, but the design and analysis, if both transducers are weighted, is more complex because the time response of the filter is the convolution of the impulse responses of the two transducers. Both of these designs require compensation for effective velocity changes under the transducer that are introduced in fabrication, for propagation losses and dispersion introduced by the electrode metal, and for scattering losses as the waves propagate under the transducer. These scattering losses are particularly severe in compression (up-chirp) filters where the high-frequency components of the signal must propagate under the low-frequency part of the transducer. Since plate-mode (or bulk-wave) velocities are higher than surface-wave velocities, the low-frequency electrodes can scatter higher-frequency surface waves synchronously into plate modes. This scattering increases insertion loss and causes spurious output signals.

These problems are eliminated in the slanted design shown in Fig. 5c. The propagation direction is the same as in the other designs. At high frequencies, surface waves are launched only at the top of the device. At low frequencies, waves are launched only at the bottom. This configuration eliminates propagation under large numbers of nonsynchronous electrodes and thereby reduces dispersion, attenuation and scattering effects. The impulse response is a somewhat complicated convolution of portions of the impulse responses of the two transducers. This complication makes precise analysis difficult, but the slanted structure eliminates the Fresnel ripple that is characteristic of transversal dispersive delay lines.

Another approach to dispersive delay lines is shown in Fig. 6. The reflective-array compressor (RAC) uses reflection of surface waves to achieve varying path length.[6] The reflection arrays consist of grooves whose reflectivity is varied by controlling their depth as a function of position along the array. Waves at all frequencies are launched by a single broadband transducer and reflected at right angles by the first reflection array at the point where the spacing of the grooves along the direction of propagation is a wavelength. As shown in Fig. 6, a second array reflects the wave back to the output transducer. The advantages of this configuration are large dispersion, since the length of the device is used twice, and very low distortion, since reflective arrays introduce minimal distortion as the surface waves propagate through them. The disadvantage is more complicated fabrication.

The RAC device has been extensively used in systems requiring large dispersion times or large bandwidths. Laboratory devices have been built with a 500-MHz bandwidth and 10 μs of dispersion.[6] Other devices have been built with up to 100 μs of dispersion, but lower bandwidths.

Fixed Correlators

Chirp devices are examples of matched filters designed to detect particular frequency modulated signals. They are

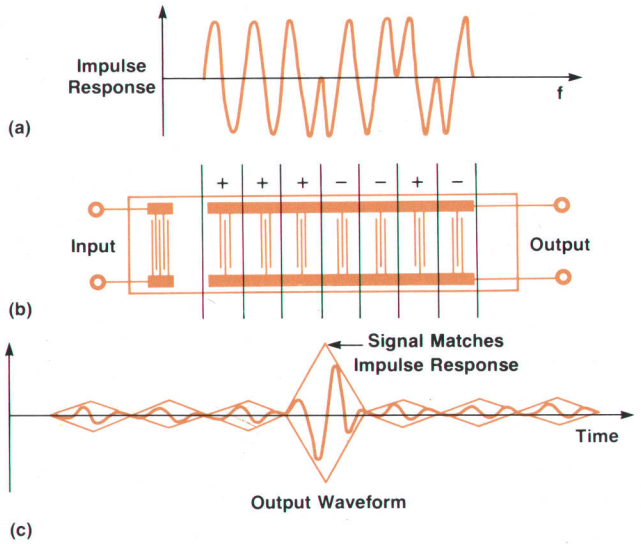

Fig. 7. *SAW implementation of a seven-bit biphase-code correlator. An incoming signal is converted into a surface acoustic wave by the input transducer in (b) and propagates toward the output transducer. When the shape of the surface wave under the output transducer matches the impulse response of the transducer (a), a correlation pulse occurs at that time in the output waveform (c).*

well suited to radar applications because the compressed pulse output is insensitive to Doppler shifts at the input and has low time sidelobes. In other applications where Doppler shift is not a problem, amplitude- and phase-modulated codes are appropriate. These fixed-code correlators can be implemented easily with tapped SAW delay lines.[7] The size of a tap (or set of electrodes) determines its amplitude and its position determines its phase. To match a known coded input, the impulse response of the SAW device is the time inverse of the waveform.

Fig. 7 shows the surface-acoustic-wave implementation of a seven-bit biphase-code correlator. The electrode connections to the summing bars determine the phase of the uniformly spaced taps. In practical systems, many other codes besides seven-bit codes are used. As the number of taps increases, performance is degraded by the attenuation caused by scattering, and by spurious signals generated by reflection. This distortion can be reduced by slanting the tapped transducer in a manner similar to that discussed for the chirp transducer (Fig. 5c). In this case, however, the energy is launched across the entire width of the device and the part of the beam intersected by an individual tap (electrode pair) affects the tap weight.

Multiphase codes can be used to advantage in communication systems to reduce multipath sensitivity. These systems are called spread-spectrum systems because the information is transmitted over a larger bandwidth than that required for the data itself. If r is the data rate and there are n taps per bit of information, then the code bandwidth is n times r. This seems to be an inefficient use of the spectrum, but since the matched filter discriminates against other signals, it should be possible to have multiple signals with differing codes share the same portion of the spectrum. The major advantage of spread-spectrum systems is the reduced sensitivity to interference from signals reaching the receiver by different paths. In a narrowband transmission system this can lead to cancellation and loss of the incoming signal. In a broadband system the signal level will be reduced, but the signal will not be lost.

The advantage of SAW devices as correlators is that they are passive, inherently synchronized, real-time processors. Digital correlators have to perform many multiplications and summations to determine when an input signal is present. To maintain synchronization, a preamble must be added to each transmission. This effectively reduces the data rate. With a SAW device this preamble can be very short if it is required at all. The radio data link described in the box on the next page is an example of a system that uses SAW devices in this manner.

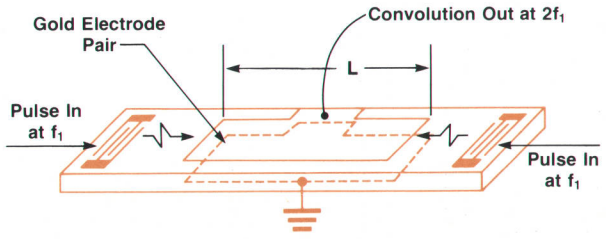

Fig. 8. *Basic configuration for SAW elastic convolver.*

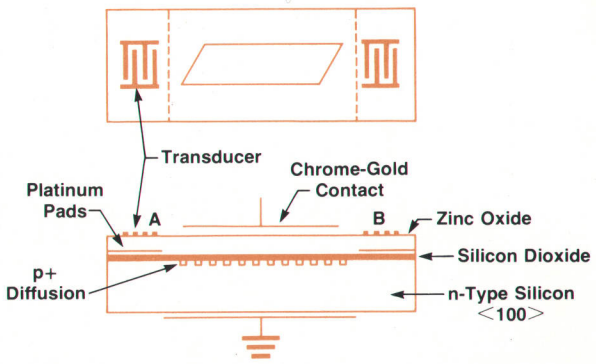

Fig. 9. *Configuration of a monolithic diode storage correlator.*

Programmable Correlators and Convolvers

The disadvantage of fixed correlators is that the code can be changed only by making a new device. If nonlinear devices are used, it is possible to make programmable correlators where the reference function encoded in the transducer is determined by an auxiliary input signal. The simplest implementation of this device is the SAW elastic convolver (Fig. 8).[8] As the reference and the input signals pass through each other, nonlinearities in the substrate generate a signal that is proportional to the product of the signals. The sum-frequency component of this product has no spatial variation and can therefore be summed by a simple solid plane electrode. This summation corresponds to an integration of the product over the length of the electrode. Mathematically this is a convolution. If the reference signal is the time inverse of a signal to be matched, the output is the autocorrelation function of that signal. Therefore, if the reference is a chirp signal, the device can be used as a pulse compressor. If the reference is a coded waveform, it behaves like a fixed correlator. The advantage of a device with this flexibility is obvious—one device can now perform a variety of functions. The disadvantages are the requirement of generating a reference signal at each convolution interval and the inefficiency that results from relying on the weak nonlinearities in the substrate to obtain the product. The fact that the reference is also a moving wave makes signal acquisition and synchronization more difficult.

The weak nonlinearity problem can be solved by introducing a semiconducting medium to do the mixing.[9] This was first done by placing a semiconducting slab in close proximity to the piezoelectric substrate. The electric fields associated with the acoustic waves extend above the piezoelectric surface and modulate carriers in the semiconductor. The voltage generated across the thickness of the semiconductor is proportional to the square of the driving electric fields, so one component of this voltage corresponds to the product of the modulation of the two input waves. The interaction in this case is much stronger than the interaction in the piezoelectric substrate. It is highly dependent on the strength of the fields at the semiconductor surface and therefore on the size of the piezoelectric-to-semiconductor gap. The interaction strength is maximized with a gap of 100 to 500 nm depending on the semiconductor properties. The size of the gap is critical because contact between the two materials results in damping and scatter-

Radio Data Link

The radio data link described here is a system for wireless data communications between a computer and several remote terminals located within a large, open building.[1] The system uses direct-sequence spread-spectrum techniques to overcome multipath interference and a SAW correlator to minimize sensitivity to signal variations and to improve signal acquisition time. This radio data communications system is designed to operate indoors over a limited range and with very low transmitted power. Such a system has two advantages over networks that use metallic or fiber-optic cables:

- A terminal may be installed wherever it is needed by putting it in a convenient place and turning it on. The need for cable installation to every foreseeable location is avoided.
- Terminals can be completely mobile and still remain connected to the network.

These two advantages make possible a variety of applications in office, warehousing, manufacturing, and instrumentation environments.

To realize these advantages fully, one must first address and overcome the problem of multipath interference. The potential for multipath interference arises when radio signals, as a result of reflections from the walls and objects within a building, reach a receiver by two or more paths of different lengths. Depending on their frequencies and relative path lengths, signals arriving by these paths may add destructively and produce deep nulls in the signal power available to a receiver. A conventional narrowband signal can suffer a loss greater than 25 dB. To overcome this loss either the transmitted power or the transmitted bandwidth can be increased. In either case more signal power reaches the receiver, but the wideband approach requires far less transmitted power for a given operating range. The system reported here uses a wide bandwidth developed by means of direct-sequence spread-spectrum techniques, sometimes called pseudo-noise or PN spread-spectrum.

To test the feasibility of using direct-sequence spread-spectrum techniques for data transmissions within buildings, three transceivers having the following characteristics were designed and built.

Data Rate:	100 kilobaud
Code Length:	255 bytes
Code Rate:	25.5 MHz
Carrier Frequency:	1.5 GHz
Modulation:	binary phase-shift keying
Bandwidth:	51 MHz
Transmit Power:	5 milliwatts
Operating Range:	300 metres

The operating range is adequate for many applications but can be increased by increasing transmitter power. For example, a range of approximately one kilometre can be expected with a transmitter power of 50 milliwatts.

Two CRT terminals and a central computer were outfitted with the transceivers. A multipoint polling protocol which used existing CPU software and terminal firmware was chosen in the interest of expediency. The transceivers were equipped with RS-232-C interfaces and appeared to the CPU and terminals as standard, high-speed, synchronous modems.

Although a microprocessor-based receiver was originally used in the system, it was replaced by a SAW-based receiver to overcome two major drawbacks. First, the microprocessor receiver was sensitive to rapid changes in multipath structure which sometimes occurred as people or objects moved about in the area where the radios were operating. Second, the microprocessor synchronism acquisition time was 100 milliseconds which severely degraded the channel throughput. These drawbacks were eliminated and a simpler block diagram resulted from the use of a SAW correlator (Fig. 1) in the receiver (Fig. 2). The incoming data is translated to the 350-MHz IF and decoded by the correlator. The data is differentially phase-shift keyed and is therefore contained in the relative phases of the compressed pulses at the correlator output. A second SAW device, a delay line with a delay of precisely one bit period, is used to achieve differentially coherent detection. A vital feature of the delay line detector is its ability to demodulate signals arriving via different paths properly even though their carrier phases are unrelated. The output of the detector is integrated during a 2-μs-wide window centered on the correlation peaks. In this way the receiver collects power from all signal paths and bases its data-bit decisions on total signal power rather than on the power from any single fragile path.

Signal acquisition time is limited by the settling time of the AGC loop to about one millisecond, which is considered adequate for the polled, two-terminal network. The polling rate is about 50 transactions per second. Reducing the acquisition time would not increase this rate appreciably. The SAW correlator results in a reduction in the signal acquisition time by a factor of 100 and thereby allows the system to operate at its full 100 kilobaud data rate.

Acknowledgments

This radio link was designed and built by Payne Freret, Ralph Eschenbach, Dick Crawford, Paul Braisted and Lyman Miller with the assistance of Zvonko Fazarinc, Hap Horn, and Frank Lee.

Reference

1. For a more detailed description of this system refer to P. Freret, R. Eschenbach, D. Crawford and P. Braisted, "Applications of Spread-Spectrum Radio to Wireless Terminal Communications," IEEE National Telecommunications Conference Record, 1980, pp. 69.7.1-69.7.4.

-W. R. Shreve

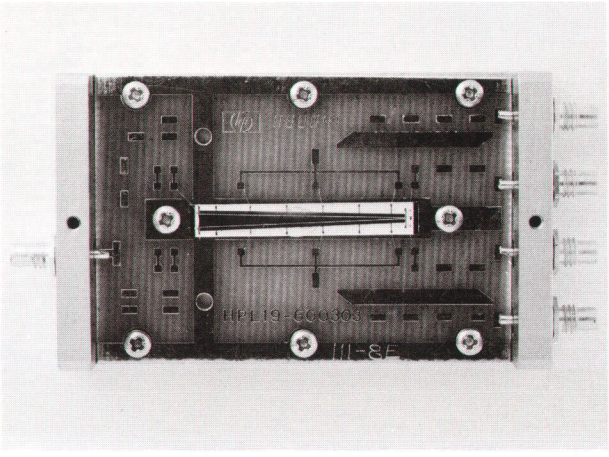

Fig. 1. *Photograph of the SAW correlator portion of the radio data link before discrete components are bonded on.*

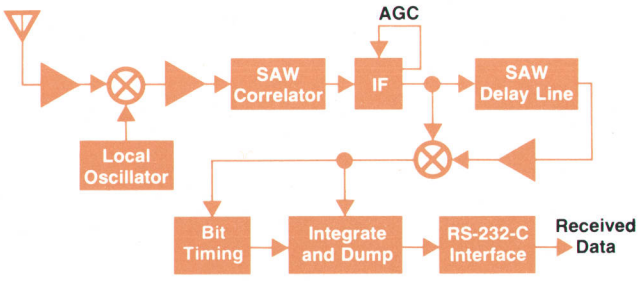

Fig. 2. *Simplified block diagram for the SAW-based receiver used in the radio data link.*

ing of the waves. Too large a gap or variations in the gap causes decoupling or variations in the coupling between the piezoelectric substrate and the semiconductor.

Substitution of a diode array for the semiconducting slab further enhances the convolver's performance and flexibility because charge can be stored in the diode array. In one mode of operation, successive convolution outputs can be added to the charge stored in the diodes to make an integrating correlator. In the normal convolution mode, the reference signal can be stored as a charge image on the diodes to alleviate the problems of continual reference generation and synchronization with a moving reference. The storage time is determined by the diodes and is typically a few milliseconds. The reference must still be refreshed, but 1000 times less often.

The difficulties in fabricating a two-substrate piezoelectric-semiconductor convolver can be bypassed by using a substrate such as gallium arsenide that is both piezoelectric and semiconducting or by depositing a thin layer of a piezoelectric material like zinc oxide on a semiconducting substrate like silicon (Fig. 9). Monolithic devices now have efficiencies and bandwidths equivalent to those obtained with separate substrates.[10]

The use of programmable SAW correlators and convolvers is currently limited to research laboratories. System applications are limited by the correlator's high loss and limited dynamic range. When the losses associated with transduction over a useful bandwidth (25%), propagation, and the interaction are combined, the ratio of the output power to the product of the two input powers is about −50 dBm. Thus if a +20 dBm reference is used, the ratio of signal-to-output power is −30 dB. This loss is more than 20 dB better than the first convolver loss reported, but it is still substantial. The dynamic range is limited by thermal noise at low power and saturation at high power and varies from 20 dB to 40 dB depending on the configuration. It limits both the useful power range at the input and the accuracy that can be achieved in the convolved output.

Summary

Surface wave technology is maturing and devices that were once confined to military applications demanding high performance, even though the cost may be high, are now being used in cost-sensitive commercial applications like television IF sections. Applications outside the military arena have been limited to simple filters and resonators. As commercial communication systems proliferate and become more complex, signal processing applications of SAW devices are becoming more common.

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William R. Shreve

Bill Shreve was born in Dobbs Ferry, New York and attended Cornell University, earning a BS degree in engineering physics in 1969. He continued his studies at Stanford University, receiving the MS (1971) and PhD (1974) degrees in applied physics. Bill joined HP in 1978 with four years of industrial experience working with SAW technology. At HP he has worked on SAW resonators and is the project manager for the SAW program at HP Laboratories. He is named as an inventor on three SAW device patents and is an author of more than twenty papers related to SAW devices. Once an instructor in the Continuing Engineering Education Program at George Washington University, Bill is the founder and vice-chairman of the Santa Clara Valley Sonics & Ultrasonics Chapter of the IEEE and a member of the IEEE Sonics & Ultrasonics Group Administrative Committee. He lives in Sunnyvale, California with his wife, two daughters, and the family dog. He enjoys jogging, hiking, woodworking, and gardening.

Retrofitting for Signature Analysis Simplified

This microprocessor exerciser provides preprogrammed external stimulus routines and monitoring circuits for signature analysis troubleshooting of microprocessor-based systems.

by Robert Rhodes-Burke

SIGNATURE ANALYSIS troubleshooting techniques have reduced the cost of fault isolation in digital circuits for many HP customers. The cost savings have accrued from the use of lower-cost equipment and personnel with lower skill levels, and from more rapid fault isolation. Over 1000 companies have purchased HP signature analyzers for testing digital logic circuits.

Signature analysis testing is used often in complex digital systems. It is frequently designed into the products, but several cases of retrofit have been successful in products not designed originally with signature analysis in mind. In general, the most effective implementations are those where some thought was given to testability considerations in the product development cycle.

Until now, existing products not designed with signature analysis in mind were not retrofitted as often as they could have been. One factor may have been the perception by production and service engineers that the retrofit process was similar to the design process and required R&D involvement. Designers are not always available to work on products already released to production, and production and service engineers may feel that they do not have the time or circuit familiarity to retrofit the product themselves. Consequently some products miss the opportunity to use this technique to enhance their serviceability.

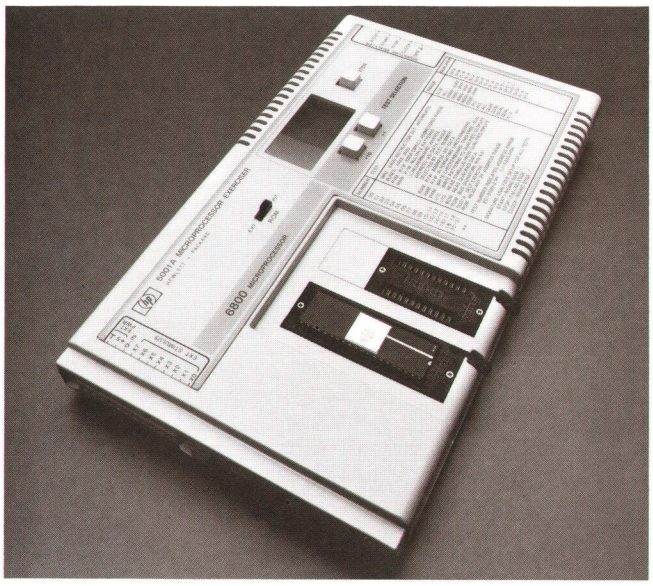

Fig. 1. *Model 5001A Microprocessor Exerciser makes it possible to apply signature analysis troubleshooting techniques to 6800-microprocessor-based products not originally designed for signature analysis methods. Other versions (5001B,C,D) test products based on the 6802/6808, 8085A, and Z80A microprocessors.*

Another point is that some minimal amount of hardware may be required to provide the timing signals to the signature analyzer. The signals required are simple in nature: start and stop flags to identify the boundary of the data stream of interest, and a clock pulse that indicates when data is valid for sampling purposes. Usually the designer can locate suitable timing signals already existing in the system. Occasionally a slight design modification, costing only a package of gates, is required. This represents some change, which can be considered intolerable in products released to manufacturing.

Thus the design-in philosophy is clearly the best, but the simplicity of the retrofit task, when viewed correctly, has not been stated strongly enough. The HP Model 5001A Microprocessor Exerciser (Fig. 1) should help remove some of the obstacles to evaluating signature analysis as a viable test alternative.

The Microprocessor Exerciser

The 5001A Exerciser makes the retrofit of signature analysis easier. The hardware impact on a product is reduced to the addition of a socket at the microprocessor location if one is not already present. The microprocessor exerciser provides a number of general-purpose preprogrammed stimulus exercises. These exercises can be adapted to a typical system with little effort. Valuable ROM space is not needed because the exerciser, acting as an external test stimulus, does not require any memory allocation concessions in the user system.

The exerciser provides signature analysis experience in products as the technique is learned. Users can begin immediately to use signature analysis in their product by connecting the exerciser to the product and selecting any of the preprogrammed stimulus programs. Thus the newcomer can actually experience the use of signature analysis before gaining an in-depth understanding of the process. Even if the user abandons the exerciser later to implement a designed-in approach, the user will benefit from the use of the exerciser and learn more quickly than by earlier

methods.

The 5001A reduces the need for R&D personnel to be involved in the retrofit of existing products. Since the programs are preprogrammed and tested by the designers of the exerciser, the service engineer has a starting library of many routines useful in exercising circuits connected to microprocessor system buses. The exerciser lets the service engineer extend the programs to cover custom circuits or unique configurations in the product under test. The ability to write functional tests is also provided. These programs can be co-resident with diagnostic signature analysis exercise programs.

Additional product hardware requirements are nearly eliminated, except for the required socket for the microprocessor and the breaking of feedback loops in the circuits beyond the processor buses. It is still true that, unless feedback loops are broken, signature analysis techniques have some difficulty in isolating a fault. However, it should be noted that the detection of a fault is not impaired. Also, this deficiency affects most board testers, which observe only edge-connector activity. Good design practices can alleviate the grief caused by this configuration, at low expense to the product, whether tested on an automatic test system or on a bench using signature analysis.

Signature analysis takes place at the normal speed of operation of the system. This is a major contribution because faults that may not show up in slower-speed test methods can be detected by at-speed testing. The fact that the testing occurs in the product rather than on some fixture adds to the near-perfect duplication of the environment that will be seen by the circuit in normal operation. This benefit is not often realized in other test methods.

A number of preprogrammed test programs are carefully developed to take advantage of other features of the 5001A. An example is the bus signature test that produces a single-measurement result in response to the eight-bit bus activity. The most frequent appliction of this test is the single-measurement verification of a product's ROM data.

The 5001A Microprocessor Exerciser is the first of a family of exercisers for the most popular microprocessors (see page 17). The characteristics of other exercisers in this family are essentially the same as described for the 5001A, which is specifically designed for the 6800 microprocessor. Some of the features of these exercisers are:

- Timing signals. All necessary timing and control signals required for a signature analyzer are produced within the circuits of the exerciser. This eliminates hardware overhead in the product under test. The timing signals are controlled by the program, whether internal or custom. This allows several programs to use dynamically varied stimulus depending upon the response of the product under test.

Signature Analysis Reviewed

In signature analysis testing, the objective is the detection and isolation of digital faults that produce incorrect circuit functions. The technique requires a repeatable stimulus of the circuit so that digital data streams are produced at various points of interconnection (nodes) within the circuit. The signature analysis test collects these bit streams in a fashion that compresses them. The compression is similar to the well-known technique of cyclic redundancy checking in data communications. The results of this compression by HP signature analyzers are signatures consisting of four hexadecimal digits. In a properly operating circuit, the signature for a given node and a given stimulus is stable and predictable.

Because signature analysis is a stimulus and response technique, effective stimulus and response-measuring instruments are required to test a given circuit or system. For response, either the HP Model 5004A Signature Analyzer or the Model 5005A Signature Multimeter provides the required measurement capability. With stimulus applied to a circuit the user probes the nodes of the circuit with one of these analyzers and compares the signatures they display with those of a known good circuit, as listed in a service manual.

An important characteristic is that testing takes place within the product, at the normal speed of operation of the circuits, unlike most board test systems. To achieve this, the product, if microprocessor based, must execute software so that the stimulus process results from the program activity. The advantage of testing at speed is obvious, but blunted somewhat by the necessity of having a subset of the circuits functional before the test can take place. This subset is often referred to as the kernel. This is the innermost layer of hardware and/or firmware required to validate the basic function of the microprocessor chip. This is often the microprocessor and its requisite clocks and power supplies.

The signature analysis test is often viewed as a diagnostic test that is used to isolate faults detected by some other means. Sometimes these means are functional or self-tests. In some implementations these means can be carefully designed signature analysis exercises that produce a go/no-go result.

The stimulus must be such that each node has a unique bit stream, and further, that the circuit elements are exercised so that the activity is an approximation of normal operation. This latter condition suggests that it is not necessary to generate all possible input states to exercise a digital circuit if certain conditions are never possible in the system. In any case the stimulus must be constructed so that a repeatable and continuous exercise of the circuits under test is provided.

Only if the stimulus is correct can the response of the circuits under test be evaluated as to its correctness. There is a simple dichotomy in the result, either the data stream was correct and produced a correct signature, or the signature was not correct. The latter case suggests a faulty data stream, and thereby detects a faulty function somewhere upstream of the data flow.

The stimulus is most often done by specially developed microprocessor programs that are executed in the product at the time of diagnosis. The stimulus programs are loops that cause repeatable digital data streams. This type of program is frequently an endless loop that exercises a functional block of circuits and then repeats. The technician or service person must be able to control the selection and initiation of these test loops so that appropriate exercises are used in the troubleshooting process. The service engineer who sets up the product for service documentation also must be able to influence the selection and effectiveness of these tests.

Timing information must be provided to indicate when the beginning and end of the test exercise occurs. Timing information is also required so that the data can be taken from the circuit under test only during the time when it is correct and stable.

- Built-in tests. Preprogrammed tests exercise the most commonly occurring elements in a microprocessor system. There are tests for ROM, RAM, and I/O devices. Several variations of the RAM and ROM tests are included to allow fault isolation to proceed quickly. Several functional tests are provided to allow single-measurement verification of major functional blocks.
- Simple to use. The user interface is very simple. Three pushbuttons control test selection and a slide switch controls the program source. The front panel reflects the nature of the exerciser with a summary of the tests and their access codes printed below the display. Connection to a product is straightforward and can be accomplished in seconds. Connection to the signature analyzer is likewise rapid, using only four wires that mate with the pod connectors of the HP analyzers.
- Test variety. Some tests are single-measurement functional tests, others are complete circuit exercisers. An example of a single-measurement test is the basepage RAM test, which produces a single signature that in the 5001A corresponds to the number of correctly functioning RAM locations in the 6800 basepage area. A complete circuit exercise is the output-port stimulus program which writes all possible patterns to any output port. The port is selected by connecting a sense line to its chip select or strobe. The program determines the location of the target port, and then exercises it exhaustively.
- Microprocessor test. A microprocessor instruction-set test is included that also cycles interrupts and verifies correct responses. The microprocessor exercise is automatically entered upon power-up so that the kernel of the product under test is validated. The test uses all but one instruction of the microprocessor, and tests each instruction for correct function. The hardware and software interrupts are also tested for correct operation. The result of the test is a single measurement which appears in the signature analyzer. A more complete test result can be achieved by probing every pin on the processor, because some pins are for outbound data or address only.
- User programmable. Users can easily supply external programs to customize the 5001A Microprocessor Exerciser to their applications. A socket is provided so that the service engineer can supply a 2048×8 EPROM containing custom test programs for a particular product. These tests can be a mixture of functional and diagnostic tests and can be selected easily in addition to the internal preprogrammed exercise programs.
- Bus signature tests. Tests are present that allow a single-measurement ROM verification independent of memory location or size. The use of the input qualifier line allows the user to execute a special bus signature program that allows data to be accepted only from locations that respond with the qualifier line in a specified state (0 or 1, depending on the test). By connecting the qualifier to a ROM chip select line, a ROM's data can be accessed regardless of its position in the memory space. This technique eliminates any need to learn the memory map of the product under test, which can be a time-consuming process. The data is processed inside the exerciser and fed serially out on a single pin in the TTL output port of the exerciser. By connecting a signature analyzer to this pin, the entire contents of a ROM of an arbitrary size and position in memory can be verified. Each bit of the data is examined and contributes to the resulting signature. The single measurement is more effective than checksum methods frequently used in ROM verification. This approach can be very useful for products that use several ROMs as options. A single measurement can verify the presence or absence of a specific option in the product.
- External stimulus port. Not every point of interest in a circuit is always accessible to a microprocessor bus. This general-purpose stimulus port allows stimulus to be applied to such points. For example, this port might be connected to a keyboard input so that all possible keystrokes can be simulated by the exerciser while the microprocessor reads such inputs. A preprogrammed routine is provided to facilitate this type of test. Several variations on this exercise can be done when the qualifier line is used.
- Qualified stimulus programs. An external qualifier allows activity in the circuit under test to signal a dynamic modification of the stimulus. As described in the previous examples, an external qualifier input line is provided that facilitates testing when the exact addresses of certain devices are not known. In the bus signature example the qualifier line is used to find the ROMs of interest so that they may be tested. Custom programs can exploit this approach to produce dynamically alterable stimulus for portions of the circuits.
- Optimized for troubleshooting. The exerciser is optimized for troubleshooting digital circuits. The programs are carefully selected to provide a useful set of general-purpose routines to stimulate system components typically found in microprocessor systems. No keying in of programs or downloading is required to use the 5001A.

How the Exerciser Is Used

The 5001A is connected to the product under test by removing the microprocessor from its socket in the product. The processor is then placed in the 40-pin ZIF (zero-insertion-force) socket on the exerciser. The flat cable from the exerciser is then connected to the vacant socket in the product. The signature analyzer is connected by placing the four wires from the timing pod of the analyzer in the connector at the right edge of the exerciser. The front panel of the signature analyzer is set up for the specified edge and polarity of the timing signals. The test setup is then complete (Fig. 2).

The user then applies power to the product under test, which also applies power to the exerciser. (The exerciser requires a maximum of 550 mA, nominal, at +5V.) The microprocessor test is selected automatically and executed after power-on. The user can place the data probe on a +5V line to verify the functionality of the processor.

The user can now call preprogrammed tests with a few keystrokes and execute the desired tests by pressing the **ENTER** button. The tests selected most frequently at power-on are the ROM and RAM tests. A convenient first test for the newcomer is the free-running address test. This places

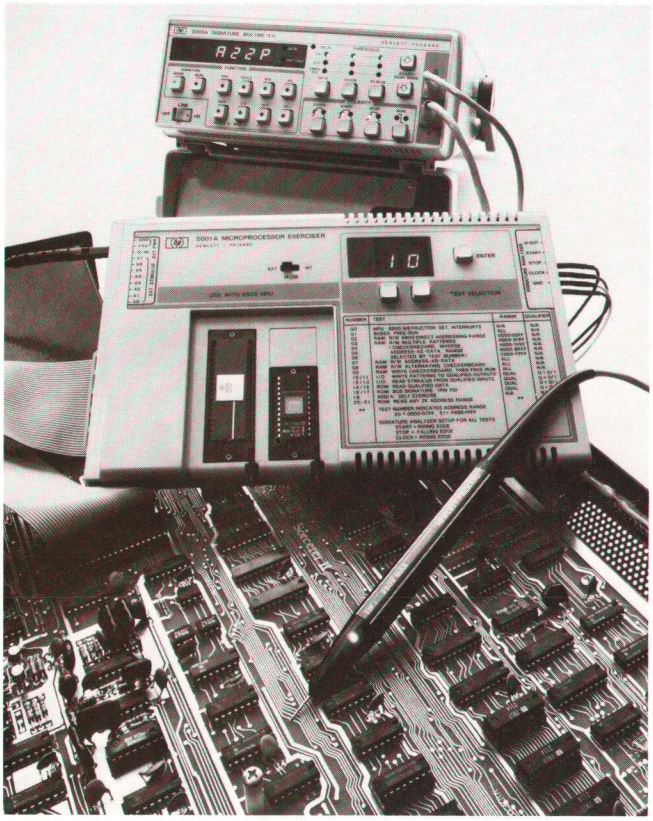

Fig. 2. *To use the 5001A, the microprocessor in the product under test is removed from its socket and placed in the socket on the exerciser. The flat cable from the exerciser is connected to the vacant socket in the product. Four wires connect the exerciser to the signature analyzer, in this case the 5005A Signature Multimeter.*

the address bus in all possible states and allows the user to validate the function of address decoding and buffers in the product.

Subsequent tests are easily selected from the exerciser front panel and executed. No restriction is made on the order of execution. Custom programs stored in EPROM or PROM also can be selected easily by the ROM-select slide switch on the front panel of the exerciser. This substitutes the external PROM for the internal ROM and allows the same degree of selection versatility.

The correct test program, of course, depends upon the product under test. There are over fifty preprogrammed stimulus programs, many of which are general-purpose. The sequence of tests should reflect the natural organization of the microcomputer portion of the product under test. The natural progression would be to start with the test of ROM either by selecting the address range appropriate to its addresses or by using the bus signature test. Then the RAM test could follow to validate system RAM. In this case either the basepage RAM test could be used or one of the half-dozen other RAM tests.

At this point it becomes more difficult to generalize about the appropriate test. Since each product has different I/O configurations, the next test selected will vary from product to product. The only general rule is to select tests that move the boundary between the known good (tested) circuitry and the unknown circuitry in a direction away from the processor bus. This corresponds roughly to the concept of "growing the kernel." Layers of tested circuits are added like the skin of an onion around the processor. The result is an increasing base of resources that can be used for test stimulus or response detection.

The I/O section can be tested to some degree by the general purpose I/O tests that are included in the 5001A Microprocessor Exerciser. There are two categories: output-port stimulus tests and input-port stimulus tests.

The execution of the selected program is straightforward—simply pressing the **ENTER** button on the exerciser will cause the program to be executed. That program will continue to execute until another program is selected and entered or power is removed. The program execution is sufficient to cause some stimulus to be generated in the product under test. The user then places a data probe on the devices being stimulated to collect data streams. The resulting data is compressed to produce a signature that can be read from the signature analyzer.

The user then compares that result to the documented result from a known good unit. The response is either correct or incorrect. A mismatch between the two readings indicates that at least some portion of the data stream in the product under test is not correct. The user then applies backtracing techniques to the circuit to locate the faulty component(s).

The test is only as good as the documentation developed by the service engineer. To develop effective documentation the service engineer must take the signature from a known good unit while it is being stimulated in the same fashion as will be used in the service environment. This is accomplished by the selection of an appropriate stimulus, application of the stimulus, and then documentation of the resulting signatures for later comparison with results from tested units.

The evaluation of a test is not finished until verification of the effectiveness of the test. This can be done by probing within a circuit in a known good unit while faults are induced. Should the test fail to detect an induced fault (such as a shorted trace) it should be analyzed to discover how it could be used better or modified to correct this deficiency. In most cases simple modifications can be made. A side effect, however, is that a new set of signatures will often result when a test program is modified.

The programs provided in the exerciser are general-purpose and not always suitable for every application of a customer. An easy means is provided so that a custom program may be run on the exerciser. An extensive user guide has been developed for custom programming. Sample programs are provided along with short tutorials on program modifications. There also is a suggested program-control routine that can be placed in the custom ROM so that the custom-test selection process can be identical to the internal program ROM.

Hardware Design

The microprocessor buses in the product under test and the exerciser are separated by buffers. This permits the detection and isolation of faults that affect address and data transfer in the product, while allowing the diagnostic pro-

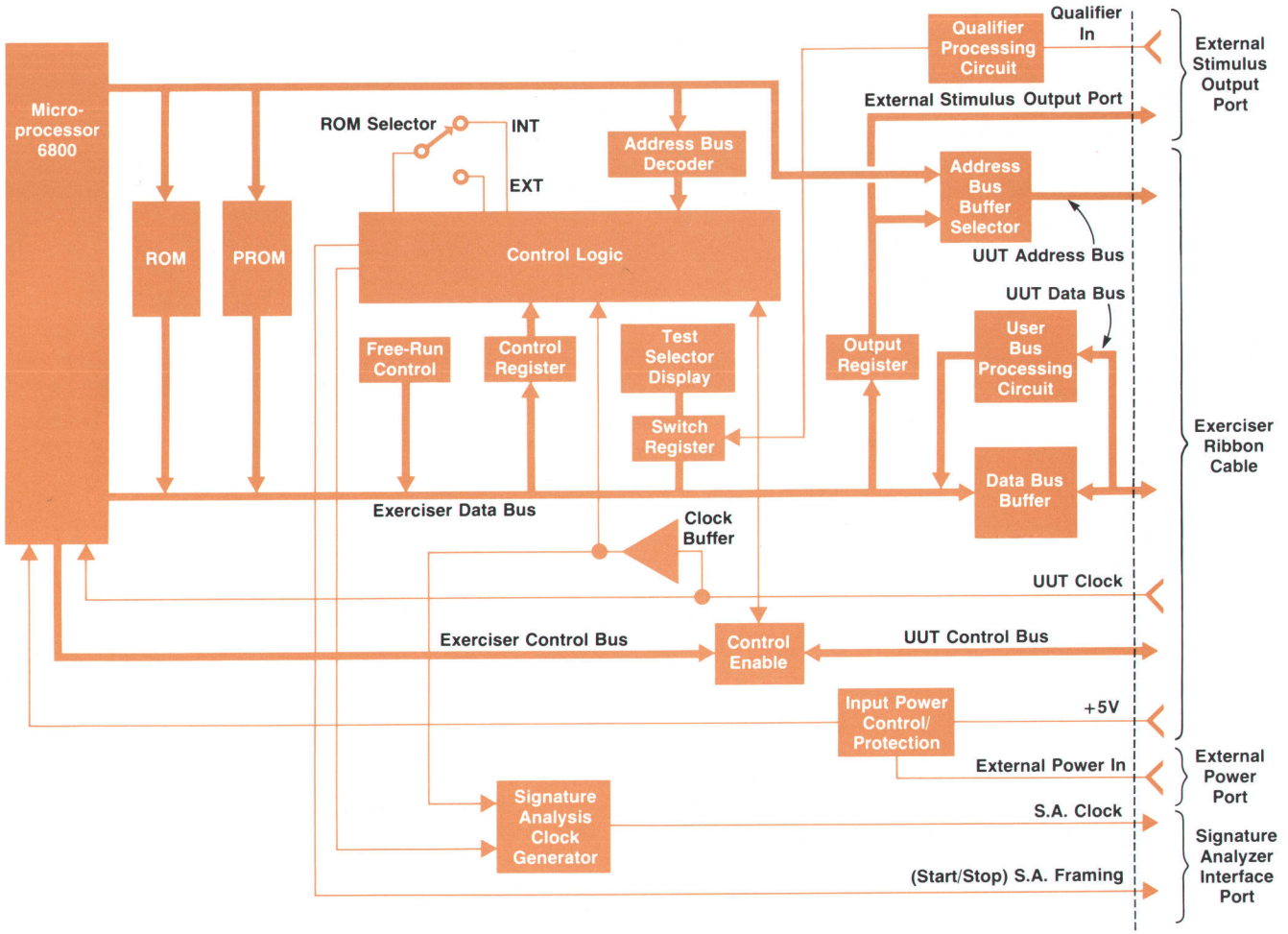

Fig. 3. *Block diagram of 5001A Microprocessor Exerciser (UUT = unit under test).*

gram to function normally. This would not be possible in some cases in which signature analysis has been designed into the product.

Fig. 3 shows a block diagram of the 5001A Microprocessor Exerciser. The user bus processing circuit can be used to monitor the data transactions in the product under test. Since simultaneous activity occurs in the exerciser and the product, it is useful to be able to capture the activity of the product data bus so that the microprocessor can, if the program is so written, test the data from the user system. The exerciser's novel data bus capture circuit allows dual address space maintenance (i.e., in the exerciser and the product) while access to data on the user's product data bus is maintained. A shift-register-like delay is introduced to capture and delay the user bus data for later access by the microprocessor. (See Fig. 4. Also see "Software Design," page 15.) Software control is maintained so that user data can be accessed or ignored at the program's option. This lets the processor access both the programs in the exerciser and the data stored in ROMs or RAMs in the product under test. The exerciser cannot, however, execute programs from the product being tested. This limitation is not serious because the programs can be validated by testing the machine code with the bus signature test. This test is not available in any signature analysis product at present. The operation of the unit in the presence of bus faults is also an improvement over earlier techniques.

An internal 2K-byte program ROM contains the preprogrammed stimulus firmware. This ROM or the user's custom ROM can be selected from the front panel. The ROM is decoded in such a way that test programs can appear to run in any location in the possible 64K-byte address space of the processor (see "Software Design," page 15 and Fig. 5a).

There is a single sense line which is processed in a manner similiar to the data bus activity in the unit under test. This line can be connected anywhere in the user's system so that TTL-level activity can be captured synchronously with the stimulus program activity. A typical use of this external qualifier line is on chip-select lines, to identify interesting sections of the address map in the system under test.

The signature analysis clock generator takes the clock signal from the processor and, after buffering in a high-speed buffer, generates a program-controlled signature-analysis clock at either the read or the write time of the microprocessor. The programs for the exerciser use the software control feature to generate the qualified clocks sent to the signature analyzer for windowing a data stream.

The hardware generation of clocks ensures that the microprocessor is in step with the data being collected by the signature analyzer. Clock skew has been minimized by a

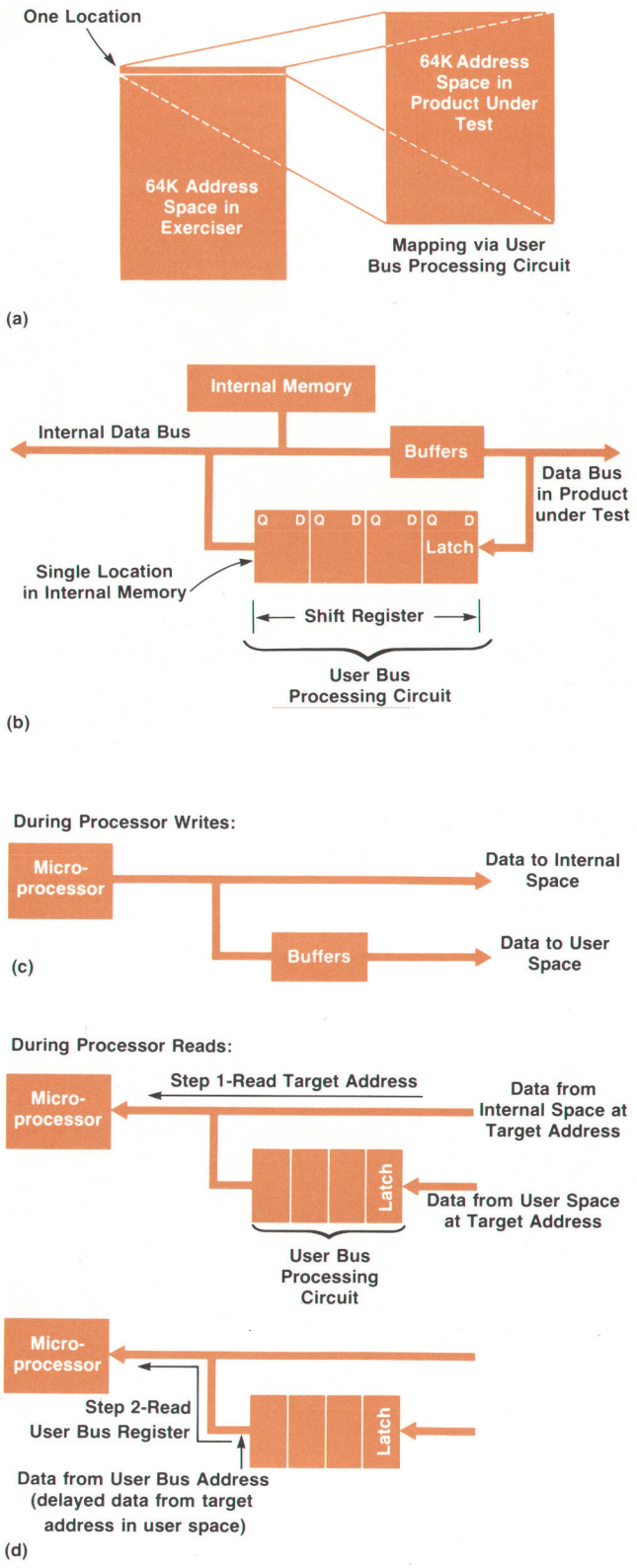

Fig. 4. *The 5001A maintains a dual 64K address space by mapping the user space in the product under test into a single location in its internal memory. The user bus processing circuit delays responses from the user memory and the microprocessor reads the delayed data by reading the single internal memory location.*

compact low-power Schottky logic implementation, and produces negligible effects in most test systems. The fact that the signature analyzer is connected to the exerciser rather than the product under test eliminates the possibility of error due to incorrect connection and simplifies testing when several products must be checked. The single setup required for all built-in programs in the exerciser eliminates another source of operator error. Because custom programs can access all features of the hardware, this single setup feature is available even in custom programs.

The control logic allows the software to control the functions of the exerciser as the stimulus programs execute. An example is placing address buffers in the high-impedence state during the microprocessor test so that address or data bus faults in the system under test cannot affect the test. Other functions allow access to internal exerciser registers and the software-induced free-run of the processor.

In the exerciser is a simplified overlay register scheme that is software-controlled. The processor executes reads or writes to internal exerciser registers by reading or writing to two memory locations. Thus the overlay register scheme has minimal impact on the address space available for programs. Unlike some input checking equipment test alternatives, the complication of a movable shadow RAM effect is not present. The two locations of the 65,536-word memory that are affected were carefully chosen and can be disabled for testing the user's system if required.

The user can make the processor free-run by executing a very short program that sets a bit in the control logic and latches the free-run state. As this occurs the internal ROM is disconnected and a CLR B instruction is connected in its place. CLR B is effectively a NOP instruction when observing processor activity externally (see Fig. 5b). For all possible addresses the processor sees an instruction whose outward effect is simply to increment the program counter and read (fetch) the next instruction (also a CLR B). The result is that the processor cycles through all possible addresses and reads continously. This is an exhaustive test of the address bus of the product under test.

Any of the 51 tests in the exerciser program memory may be selected by pressing two switches on the front panel. The value of the two digits displayed is available to the processor by reading a switch register. This is usually done only during the reset that occurs after the user presses the **ENTER** button to indicate that the selected test number is to be executed. Whenever the switch register is modified the decimal points in the display are lighted to indicate a possible mismatch between the test currently executing and the number in the display. This condition is cleared when the **ENTER** button is pressed.

The external output port is an eight-bit latch that can be accessed and updated at any time by the program. This port provides stimulus signals for circuits beyond the reach of the processor bus at a rate synchronous with the stimulus program. This allows testing some circuits that need initialization, require external inputs (such as keyboard), or run asynchronously with the microprocessor bus (such as the handshake line into a parallel interface device).

The exerciser requires that the product under test supply an additional 550 mA at 5Vdc ± 5%. If this cannot be provided through the microprocessor socket, the exerciser

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e. Reliable supplier _____
f. A broad line of products _____
g. Technically advanced _____
h. Good company to work for _____
i. Corporate citizenship _____

14. Of all the periodicals (magazines and trade journals) you read, please list those that are most important to you.

_____

_____

15. Please list other publications that you consider comparable to the HP Journal as sources of technical information.

_____

_____

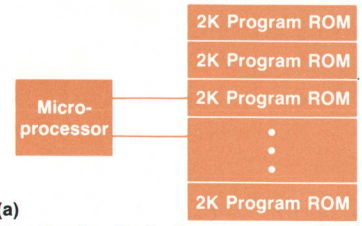
16. Please circle your area of specialty:
(circle one number)

1. Research
2. Development Engineering
3. Product Management
4. Project Management
5. Production
6. Marketing
7. General Management
8. Other _____

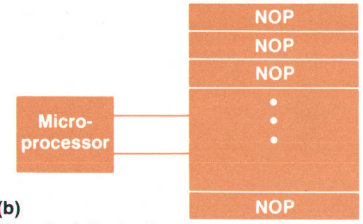
Thank You

can use an external power supply. When the supply is connected to the external power input lines, its presence is detected automatically and an internal relay disconnects all logic except the microprocessor and a low-power clock buffer from the system under test. The relay actuates so that the external supply can absorb virtually all the extra load required by the exerciser. An additional advantage of this technique is that the exerciser can be used even when power supply margin tests are run on the product under test. The microprocessor always runs from the power supplies of the product being tested.

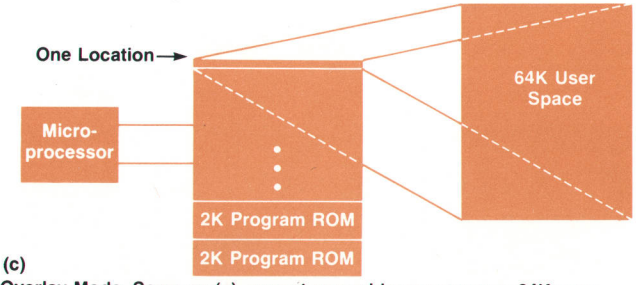
Protection circuits are built into the exerciser so that reverse voltage on the external supply will not actuate the relay, thus protecting the exerciser from damage. An overvoltage protection circuit is also included. If overvoltage occurs, an internal power Zener diode will avalanche, blowing an internal fuse. This fuse is socketed for easy replacement. The fuse also provides overcurrent protection.



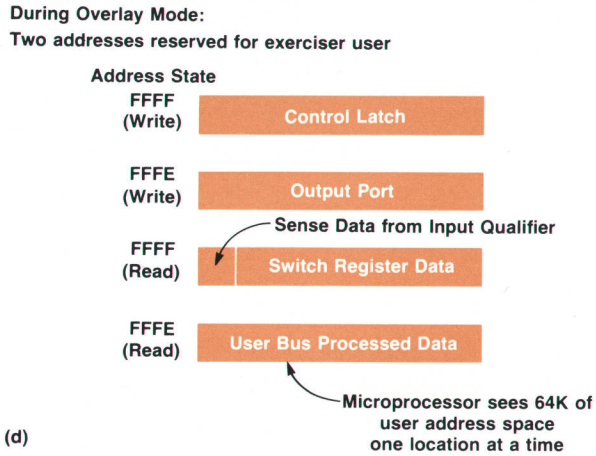
(a)
Non-Overlay Mode. Processor sees 32 identical 2K × 8 ROM images.



(b)
Free-Run Mode. Processor sees 64K filled with NOP instructions.



(c)
Overlay Mode. Same as (a), except one address accesses 64K user space and one address accesses switch register.



(d)

Fig. 5. *5001A operating modes.*

Software Design

The memory mapping scheme allows versatility in test location. The internal preprogrammed stimulus routines reside in a 2048×8 ROM. The decoding of this ROM allows the individual routines to appear to run in any of the thirty-two 2K× 8 pages of memory. The ROM images itself into these pages by ignoring the five most-significant address lines in the ROM decoding. The result is that a stimulus program can be made to overlay any page in the memory space of the product under test. The user data bus processing circuit assures that data streams resulting from instruction fetch in the stimulus programs do not interfere with the interleaved data streams resulting from instruction execution (the stimulus).

The user data bus processing circuit represents an unusual, but effective, way to access data occurring simultaneously on two buses without resorting to an elaborate mapping or clocking scheme. The situation is one wherein two 64K address spaces are mapped into one that can be read by a conventional 16-bit-address-bus microprocessor. By mapping the user's addressable space into a single location, then overlaying that single location into the internal address space, great economy in hardware was achieved. Figs. 4, 5c, and 5d illustrate this overlay mode. The user data processing circuit captures the data at the end of an instruction cycle just as the microprocessor would. It latches the data on every machine cycle, and then presents the data to a four-level eight-bit-wide shift register. The output of this register is decoded as if it were a single address in the address space of the internal bus. The address chosen overlays a location that is very infrequently accessed by the internal programs. The location selected is the reset vector (note that a reset pulse will cause the ROM to be accessed instead of the shift register). Thus, to access any location in the user space the program simply reads from the location desired, and then reads the shift register output in the following instruction. The time delay introduced by the shift register is a function of the number of machine cycles required to read the register. The dual bus structure causes two sets of data to be present for every valid address: ROM or register data in the exerciser, and the product response in the user's data bus. The technique simply ignores the internal data and reads the delayed response from the user bus. The hardware overhead is only four packages, since timing and decoding signals are already present.

The microprocessor instruction set test represents a new departure in testing. The test is essentially a functional test of the instruction set. A sequence of instructions is executed that constantly checks the effect of instructions as they are executed. If at any point an instruction produces a faulty result, a branch is made to a "skip-chain" that terminates the program early, reducing the time interval of the test. Since the test is executed in a loop with signature analyzer start and stop timing emitted at the extremes of the loop, probing +5Vdc will produce a single measurement unique

to a given loop time (with 99.998% probability). The exercise is so constructed that tables in ROM are frequently used in computations, and a simulated stack is used for extensive branching and jump testing. The mapping feature of the ROM as described above is useful in this regard. The program tests all instructions except the WAIt-for-interrupt instruction. The program writes patterns to addresses that cannot be checked with the loop-length method so that a complete test result is obtained with probing of address and data bus lines during the test.

The test has another unusual feature: the real-time test of interrupts. With a stack simulated by tables in ROM, the program writes patterns to the control logic in the exerciser that cause interrupt lines on the processor to be toggled. Various tests of maskable and nonmaskable interrupts are performed, including the correctness of the transfer of control to the appropriate service routine. The fact that the interrupt lines to the user system are intercepted is essential for this test, as well as for the general stimulus programs. The microprocessor test is executed at the speed of normal operation by using the normal clocks and power supplies in the product under test, thereby performing a true kernel test in the product. The only drawback in this test is that fanout and timing tests are not made on the unit. However, the advantage that the actual microprocessor in the product is used should not be overlooked. A limitation of the input checking equipment approach, for example, is that the processor is emulated, rather than exercised.

Since the 6800 instruction set uses relative branching as a means of transfer of control within a program, position-independent code can be written. Some internal preprogrammed stimulus programs can be relocated to appear to run in other address spaces because they are written with relative branches to do looping. The advantage of this approach is the flexibility gained as custom programs are developed.

An HP Model 5004A Signature Analyzer or 5005A Signature Multimeter can be used as a remote display. This feature, which can be useful in some applications, was implemented for the testing of the 5001A. Because the program can control the start and stop and clock of the signature analyzer, a clever programmer can "finesse" a signature into the display. This occurs if +5Vdc or all logic ones are clocked into the signature analyzer when a finesse-type program is running. If the programmer knows ahead of time the number of clocks required to produce the desired signatures, then a simple loop can be set up to produce the desired result. The initial application was such that the result of a functional test produced the finesse signature of PA55 which also could be easily interpreted as PASS. Other failures are identified by signatures of FA01, FA02, FA03, et cetera. These results represent failure at test 01 and so forth. The advantage here is that a functional test can detect a fault and isolate it to a functional block such as a particular printed circuit board before diagnostics are run for that failure. The 65,535 unique signatures available open a variety of possibilities.

Product Design

The 5001A case is injection-molded glass-filled polycarbonate. The case is designed to be used with a family of microprocessor exercisers. Hence, the model can be designated by providing a different front-panel overlay for each instrument in the family.

All the nonelectrical parts are made from polycarbonate: the case (two halves), the stimulus connector, the signature analyzer connector, and the overlay panel. The use of polycarbonate makes the instrument very durable and nonconductive, two important features in the environment where the 5001A is used.

Acknowledgments

The author would like to thank Gary Gordon for his leadership and help in the early stages of the development. Gary proposed the first microprocessor stimulus product at the same time the author had implemented a similar test approach for the HP 2804A Quartz Digital Thermometer in another HP division. Andrew Stefanski contributed to the generalization of the external stimulus concept. Ken MacLeod contributed to the development with innovative suggestions and guidance, particularly with an internal design review process that was very effective.

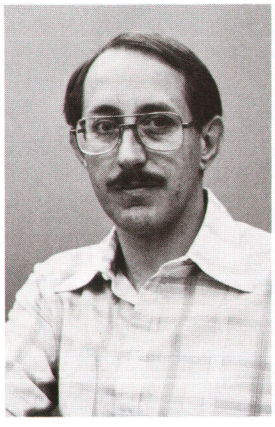
The development team grew to several people working on parallel product developments. Bob Welsh developed an 8085 version, Waymond Fong developed the Z80 version, and Dave Rick developed the 6802/6808 version. All of the designers were particularly innovative and made individual contributions to their own products as well as to the other versions. Many of the powerful test capabilities of the microprocessor exerciser came from this cross-fertilization process.

The package design, done by Dave Rueda, was specifically targeted at a family of products, providing features that allow use of the package for several products.

References

1. R.A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, May 1977.
2. H. Nadig and G. Gordon, "Hexadecimal signatures identify trouble spots in microprocessor systems," Electronics, March 3, 1977.
3. R. Rhodes-Burke, "Applying signature analysis to existing processor-based products," Electronics, February 24, 1981.

Robert Rhodes-Burke



Bob Rhodes-Burke was project manager for the 5001A Microprocessor Exerciser. With HP since 1974, he has also developed automatic test system software and digital hardware for the 2804A Quartz Thermometer. Born in Riverside, California, he served in the U.S. Navy as an electronics technician and received his BSEE degree in 1975 from California State University at San Jose. He teaches microprocessor programming at a local community college and is interested in alpine skiing, California wines, personal computers, and science fiction. Bob is married and lives in Redwood City, California.

A Family of Microprocessor Exercisers

The 5001 Microprocessor Exerciser family includes three models in addition to the 5001A described in the accompanying article. Model 5001A is designed to test products based on the 6800 microprocessor. Models 5001B, 5001C, and 5001D do a similar job for products based on the 6802/6808, 8085A, and Z80A microprocessors, respectively.

5001B Tests 6802/6808

The 5001B Microprocessor Exerciser (Fig. 1) is intended for use with the 6802 and 6808 microprocessors. Because these processors are code-compatible with the 6800, the preprogrammed stimulus routines of the 5001B are identical to those for the 5001A. The 5001B hardware resources are compatible with the 5001A so that custom test routines written for the 5001A will run in the 5001B without modification. To maintain software compatibility, the on-chip RAM in the 6802 microprocessor is disabled by the 5001B.

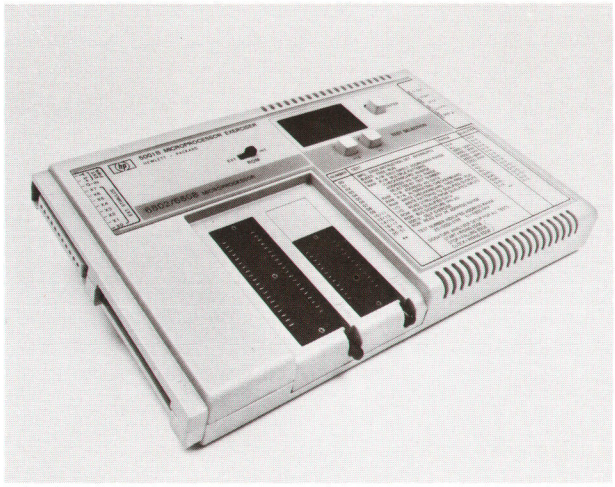


Fig. 1. *5001B Microprocessor Exerciser for 6802/6808-microprocessor-based products.*

5001C Tests 8085A

The 5001C (Fig. 2) is similar to the 5001A, with the following exceptions:

1. *Internal/External Clock.* The 8085A is different from the 6800 in that the 8085A has two basic modes for the clock function: a clock can be inserted from an external oscillator (pins X1 and X2), or the microprocessor can act as its own oscillator when a crystal, inductor, or resistor and capacitor are correctly connected to the X1 and X2 pins. The 8085A has a clock output pin that goes to the rest of the system under test (SUT). The first mode is no problem for the 5001C but the second mode poses a problem when a crystal and the 8085A are separated by 21 cm of flat ribbon cable. Sometimes oscillations occur at the residual-RC-determined frequency (usually about 20 times lower than the desired crystal frequency). Several solutions were investigated with the choice being an INT/EXT clock driver switch. In the EXT (external) position the X1 and X2 lines are connected directly from the 8085A to the corresponding pins in the SUT. The INT (internal) position connects a 4.00-MHz crystal directly to the X1 and X2 pins of the 8085A and disconnects the corresponding lines to the SUT. The INT position is guaranteed to work at 4.00 MHz (this was determined to be a frequency where most 8085A systems will operate), while the EXT position provides "at speed" operation. ("At speed" means that both the 5001C and the SUT will operate at the frequency determined by components in the SUT.) The switched clock driver solution also provides some added benefit in that the 5001C can operate in a stand-alone mode without a clock source; only a power supply is needed. Incoming inspection of 8085A microprocessors and easier service procedures are examples of the benefit.

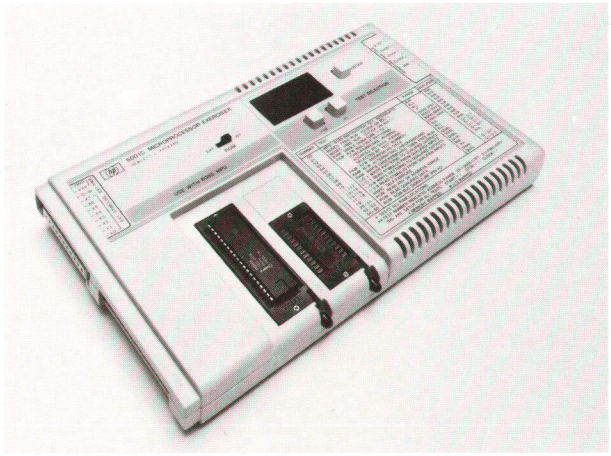


Fig. 2. *5001C Microprocessor Exerciser for 8085A-microprocessor-based products.*

2. *Multiplexed Address/Data Bus.* The 8085A microprocessor has the lower eight bits of addresses multiplexed with the eight bits of the data bus. This allows the microprocessor to have more features, but also requires more traces on the printed circuit board when the 8085A is used with standard nonmultiplexed components (ROM, buffers, etc.) Therefore, a fine-line board (0.25-mm traces with 0.25-mm spaces) is used in the 5001C. This is one of the first full production uses of fine-line board layout and fabrication in an HP product, continuing a trend towards denser printed circuit boards. The multiplexed bus also creates a need to verify signatures at two different times on the bus. For this purpose two free-run tests are used, one clocking the signature analyzer when the address is valid and another clocking the analyzer when the data is valid (more on this later).
3. *Multi-Interrupt.* The 8085A has five different interrupt pins with various levels of priority and masking. The external stimulus lines are looped to the 8085A interrupt lines through a multipurpose (also loops SID and SOD lines) buffer internal to the 5001C. This is done for test 00. The software is somewhat tricky because there is no RAM in the 5001C. In this case each interrupt triggers the next interrupt in addition to verifying masking and priority functionality.
4. *Signature Analysis Clock Generation.* Reads and writes in a microprocessor system are controlled by two factors: the state (read or write or neither) and the edge (i.e., data valid). In the 6800, state control is done by one set of lines while the clock edge is always provided by another control line, $\phi 2$. In the 8085A each separate task has its state and timing information on a separate control line ($\overline{RW}$ for reading, $\overline{WR}$ for writing, and ALE for latching addresses). This is a problem when trying to generate one signature analyzer clock signal (with minimum propagation delay) as a combination of all three control lines ($\overline{RW}$, $\overline{WR}$, and ALE) in addition to various other state-sensitive 5001C control lines. The solution is Schottky combinatorial

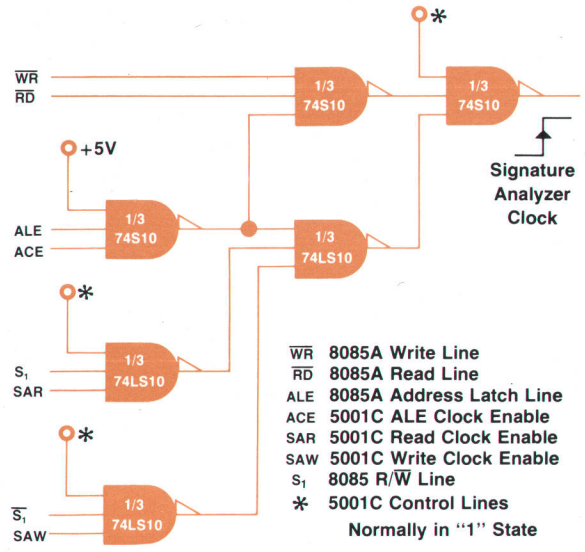


Fig. 3. *5001C signature analyzer clock generation.*

logic, keeping the delays to a minimum but still preserving the single connection of the signature analyzer clock line (Fig. 3).

5. *I/O and Memory-Mapped I/O.* The 8085A microprocessor has two modes for I/O (input/output): I/O-mapped (IO/$\overline{M}$ line = 1) and memory-mapped (IO/$\overline{M}$ line = 0). The memory-mapped mode is the normal 64K-byte address space used for memory and some I/O devices, whereas the I/O-mapped mode is a 512-byte (256 read and 256 write) address space used for access to I/O where speed or program memory space is critical. Memory-mapped I/O is more general-purpose but usually slower, while I/O-mapped I/O is less flexible but quicker. The fact that the I/O-mapped mode is not very flexible poses problems when trying to write general-purpose stimulus tests. Our solution is memory-mapped reads and writes that appear I/O-mapped to the SUT. This is not as straightforward as it seems, in that it required tricky latching of the 5001C control lines in addition to some gating of the signature analyzer clock to guarantee stable signatures.
6. *4K ROM with Paging Scheme.* The 5001 series uses an internal 2K ROM overlayed into the entire memory space 32 times such that the microprocessor sees the ROM at any address (excluding special control addresses). In the case of the 5001C, a 2K ROM is not sufficient, so a 4K ROM is used. To preserve the 2K image, one of the 5001C control lines is used to map between halves of the 4K ROM (Fig. 4). This mapping is invisible to the SUT.
7. *Comprehensive RAM Test.* Because it has more ROM space, the 5001C includes a comprehensive RAM test. This test writes a pattern to all of memory (64K). Then memory is read one byte at a time, and if the correct pattern is read, a walking ones and walking zeroes pattern test is performed to that byte. Upon successful completion of this byte test, the signature analyzer clock is toggled once and the next memory location is tested. This test essentially counts the number of good RAM cells in byte increments. An advantage of this test is that no prior knowledge is needed of where RAM exists.

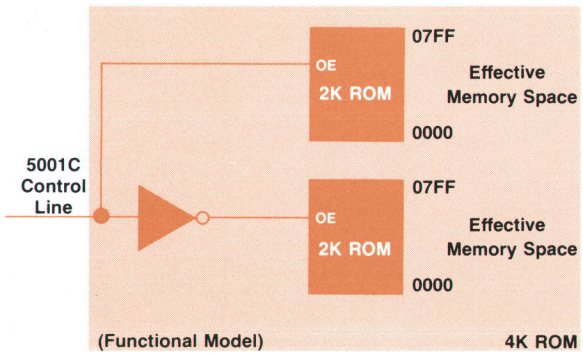


Fig. 4. *Mapping between halves of the 4K ROM in the 5001C.*

5001D Tests Z80A

The 5001D Microprocessor Exerciser (Fig. 5) is designed to work with the Z80A microprocessor. It is very similar to the 5001A Microprocessor Exerciser except for the following features:

1. *Full Instruction Set Testing.* The 5001D performs a test on the full instruction set of the Z80A. The testing of some of the instructions created interesting problems. The HALT instruction posed the problem of how to get the Z80A out of the HALT mode after its execution. This similar instruction is not tested in the 5001A and 5001B. The solution is to feed back the $\overline{\text{HALT}}$ output to the $\overline{\text{NMI}}$ input (Fig. 6). The $\overline{\text{NMI}}$ creates the interrupt, which brings the Z80A out of HALT. Another testing problem occured with the RST 0 instruction. Location 0000 had to be reserved for the 5001D power-up and manual resets, so this same location could not be used for the RST 0 jump. The solution was to use a 4K ROM that can be accessed in two 2K pages, as in the 5001C. Now the RST 0 instruction can be tested using location 0000 in the top 2K page of the 4K ROM while the 5001D resets can use the bottom 2K page. Finally, since the 5001D contains no RAM, all instructions involving stacks are done using simulated stacks stored in the ROM.
2. *Interrupts and Bus Control Testing.* During the instruction set test (TEST 00), interrupts and bus control signals are simulated to test their operation (Fig. 6). The interrupts are tested by setting the $\overline{\text{INT}}$ or $\overline{\text{NMI}}$ line low using a controlled feedback tap from the external stimulus lines. When these lines are set low, the processor is checked to see if the appropriate interrupt actions are taken. Some of the interrupt modes require external data. The 5001D has a register that sends the appropriate interrupt acknowledge response to the processor. The testing of bus control lines ($\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$) is performed by setting the $\overline{\text{BUSRQ}}$ input with a feedback tap from the external stimulus lines. The $\overline{\text{BUSAK}}$ signal generated from the processor is used to clear the external stimulus register to bring the processor back out of the high-impedance state.

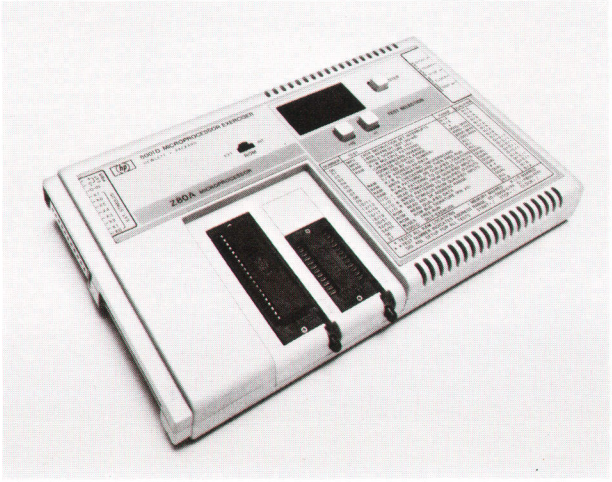


Fig. 5. *5001D Microprocessor Exerciser for Z80A-microprocessor-based products.*

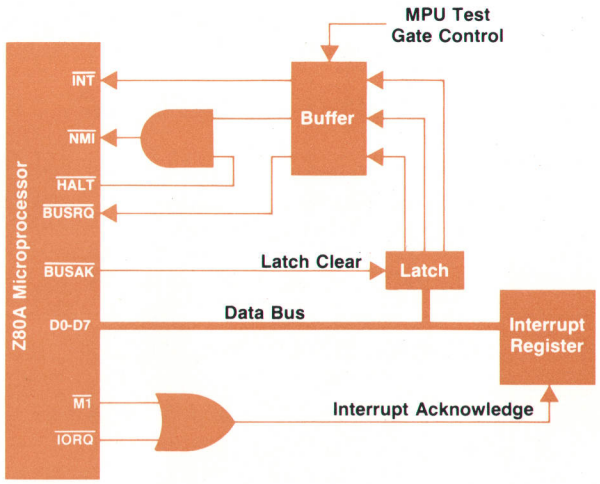


Fig. 6. *Interrupt and control signal simulation in the 5001D.*

3. *Qualified RAM Test.* In addition to the comprehensive RAM test in the 5001C, the 5001D also contains a qualified RAM test. This test allows the running of a write/read RAM test on one memory chip at a time by placing the qualify line on the chip-select signal of the RAM chip of interest. This feature enables the user to find a faulty RAM chip quickly when the other RAM tests show that there is a problem in RAM.
4. *Z80A RAM Refresh.* The transparent RAM refresh capability of the Z80A processor is preserved in the 5001D by having the refresh addresses and control signals automatically output from the 5001D to the system under test. This prevents the loss of RAM data even if the 5001D is operating independently of the system under test, with its buffers inactivated (the buffers can be turned on and off under software control).
5. *RAM Refresh Signature Analyzer Clocking.* The testing and troubleshooting of dynamic RAM systems is facilitated by giving the 5001D the ability to create signature analyzer clocks on refresh cycles of the Z80A. The Z80A refresh test (TEST 01) will test a processor's refresh capability. It can also be used to test a system's refresh decoding circuitry since the signature analyzer clocking occurs only on the Z80A refresh cycles.
6. *Fetch Cycle Signature Analyzer Clocking.* As in the 5001C, most of the signature analyzer clocks from the 5001D are created by gating the $\overline{RD}$, $\overline{WR}$, $\overline{MREQ}$, $\overline{IORQ}$, and $\overline{RFSH}$ control lines from the processor to the signature analyzer clock output. The signature analyzer clock edges from the 5001D follow the edges of these control lines. However, the fast Z80A fetch cycle prevents the use of this method for signature analyzer clocking on instruction reads. The end of the fetch cycle occurs too close to the disappearance of the address information to obtain stable signatures. To solve this problem, a sequential timing circuit was designed that gates the Z80A clock to the signature analyzer clock output. This gating occurs only at the end of a fetch cycle and only when the processor is not in a WAIT state. This method allows the signature analyzer clock edge to occur before the address and data information is removed from the system. Gating the clock into the 5001D required a low-load, fast clock buffer. A discrete transistor inverting buffer was designed to accomplish this.
7. *Shielded Flat Ribbon Cable.* A special shielded flat ribbon cable is used between the 5001D and the system under test. This cable consists of two 40-line flat ribbon cables that have every other line grounded at both ends. The cable shields the fast Z80A clock from other signals and lowers the ground impedance between the 5001D and the system under test. This allows the 5001D to operate at normal Z80A system speed.

-David Rick
-Robert Welsh
-Waymond Fong

A Fast, Compact, High-Quality Digital Display for Instrumentation Applications

Small size, low cost, and a simple digital interface make it easier for designers to build this directed-beam CRT display into their electronic instruments.

by Kunio Hasebe, William R. Mason, and Thomas J. Zamborelli

HIGH-QUALITY GRAPHICS in a compact, low-cost module are made available to instrument designers with the Hewlett-Packard Model 1345A Graphics Display (Fig. 1). This new digital display produces vector graphics on its display screen in response to digital commands from a host processor. Thus it is no longer necessary for the instrument designer to custom-design the complex circuitry needed to convert digital coordinate and character data into the analog signals required by a traditional analog X-Y display. The 1345A is a self-contained graphics display module that interfaces to a user's system as a peripheral via a 16-bit digital bus, compatible with popular microprocessors.

The 1345A Graphics Display is a 16-cm-diagonal electrostatic CRT display module containing a vector processor, optional vector memory, built-in character generator, stroke generator, high-voltage supply and deflection amplifiers. It features random vector drawing, producing bright, smooth lines, and it offers four programmable line styles, four programmable intensity levels, and a full ASCII character set with a choice of four programmable sizes and four orientations. In addition, the user may incorporate special characters or symbols by means of an auxiliary ROM. A 4K-word internal vector refresh memory is available as an option.

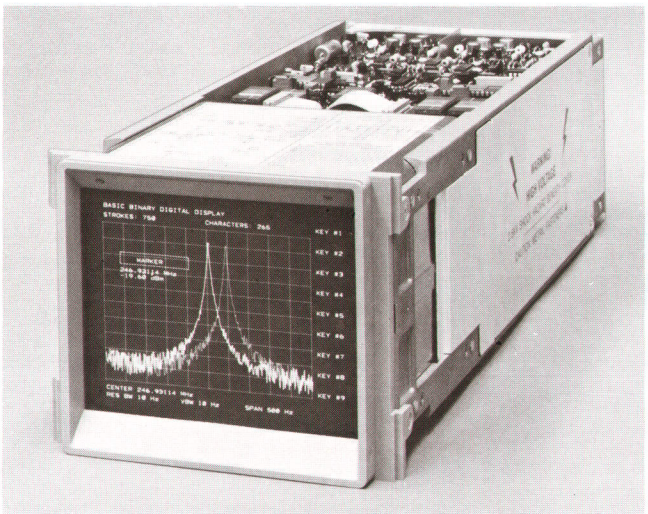


Fig. 1. *Model 1345A Digital Display Module is a 16-cm (diagonal) electrostatic CRT display component for instrumentation and measurement systems. It has high resolution (2048 × 2048 points), internal character generation, and programmable intensity and line type.*

Because of its high resolution (2048 × 2048 addressable points), the 1345A can draw both straight and curved lines (curvilinear vectors). Curved lines are drawn as a series of connected short straight vectors.

The 1345A draws all vectors in a picture by moving its display beam at the same speed. This constant writing rate insures a picture of uniform brightness (short vectors do not become brighter than long vectors).

Erasing a waveform that intersects other waveforms (vectors) does not leave blank spaces at the intersections.

At its fastest drawing rate, and at a 60-Hz refresh rate, the 1345A can draw a picture that contains up to 8194 centimetres of vectors. If the refresh rate is slowed to 40 Hz (possible in some applications), then the picture can contain up to 12,288 cm of vectors (Fig. 2).

The 1345A is intended to be integrated into instrumentation or measurement systems such as spectrum analyzers, network analyzers, and waveform analyzers. The compact display module is designed to provide an easy mechanical and electrical interface to a user's system. The entire module takes up slightly more space than the CRT envelope itself (see Fig. 1). Printed circuit boards are attached to the diecast frame with screws and are easily accessed for servicing while the instrument is powered-up. A built-in test ROM writes a self-test pattern on the screen whenever the digital interface cable is removed for servicing (see Fig. 3). The test pattern exercises all of the display module's capabilities for quick verification of operation and diagnosis of possible malfunctions.

Directed-Beam Vector Display

Much has been written comparing the advantages and disadvantages of the various CRT display techniques (see box, page 24). The 1345A uses the directed-beam, random-scan technique. It draws a line by moving the writing beam continuously between two end points at a constant rate. This produces a smooth, continuous and uniformly bright line. This compares to the raster-scan technique of drawing a line pixel by pixel. Depending upon the total number of pixels on the screen and the direction of the line drawn, the line may look jagged (Fig. 4).

In the 1345A, each vector is specified by a starting point, a stopping point, a vector speed (four different constant writing rates), and a brightness level (three different levels). To draw a picture consisting of uniformly bright lines, all lines

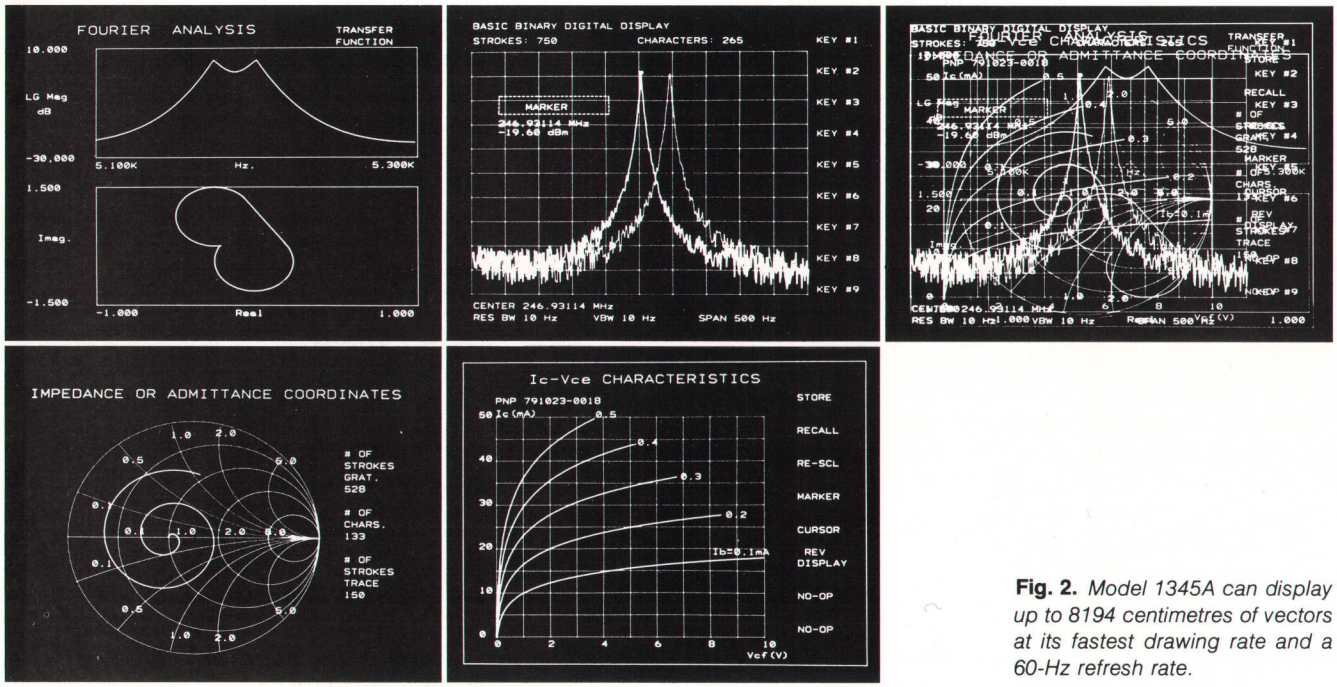


Fig. 2. *Model 1345A can display up to 8194 centimetres of vectors at its fastest drawing rate and a 60-Hz refresh rate.*

must be programmed to have the same writing rate and intensity level. To highlight certain elements of a picture, different intensity levels may be used. For example, a dim graticule might be displayed with two data traces, one bright and one slightly less bright. To vary the intensity of a trace, all that is required is either a programmed intensity level change or a programmed writing rate change. In all, twelve levels of brightness can be obtained by choosing combinations of one of the four writing rates and one of the three brightness levels (Fig. 5).

The image is maintained by being completely redrawn at approximately a 60-Hz refresh rate. Thus the picture must be stored in a refresh memory, either the optional internal refresh memory or system memory dedicated to refreshing the picture. The directed-beam technique has fast picture updating capability because only the vector end points need to be changed. This compares to the raster technique that takes time to calculate intermediate points on a line and whether a pixel shared by two lines can be erased or not. Therefore, the 1345A is capable of displaying animated pictures with ease, such as mechanical deflections in a finite-element model of a structure, or scrolling of data traces.

System Interface

As previously stated, the 1345A communicates with its host system over a 16-bit parallel data bus. The logic levels are standard TTL positive logic levels. Data is transferred using a two-wire handshake. When the 1345A is ready to accept new data, it will pull the RFD (ready for data) handshake line to the active low level. The system must then make the data valid on the data bus and pull the DAV (data available) handshake line to the active low level. The 1345A will then signify its acceptance of the data by returning RFD to the inactive high level. When the system returns the DAV line to its inactive high state, a handshake cycle is complete. Since the data transferred must be acted upon by the 1345A

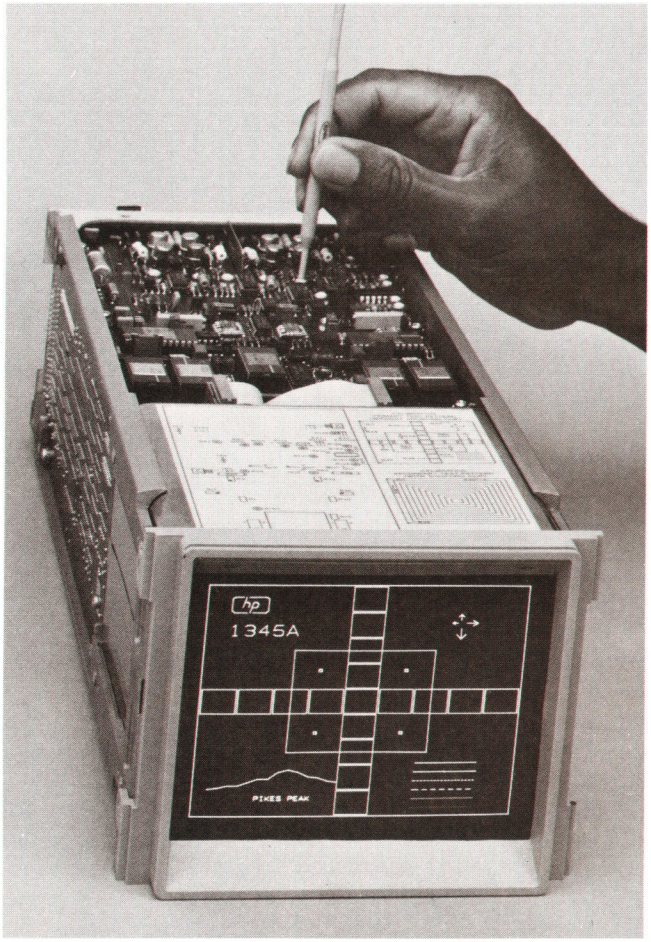


Fig. 3. *A built-in test ROM writes a self-test pattern on the screen when the digital interface cable is disconnected. A chart on top of the module shows which components to adjust to correct various parts of the pattern.*

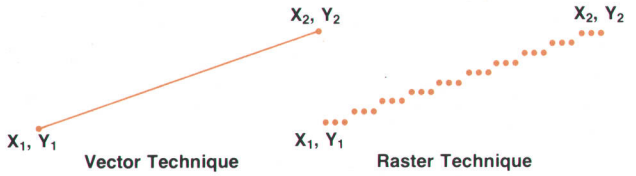


Fig. 4. *Comparing vector and raster line-generation techniques.*

before the next data word can be accepted, the data transfer rate is variable and depends on the data being sent. The data transfer rate can vary from 2 MHz for PLOT-X data to 8.33 kHz while a long vector is being drawn.

The 1345A recognizes four commands. Each command is identified by the condition of the three most significant bits on the data bus.

D15	D14	D13	Command
0	0	0	Plot Absolute
0	0	1	Graph
0	1	0	Text
0	1	1	Set Condition

The set condition command controls the beam intensity level, the linetype, and the writing speed of all vectors drawn on the CRT until another set condition command is received. The format of the command is as follows:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	I1	I0	0	0	L1	L0	0	0	W1	W0	0	0	0

I1	I0	Intensity
0	0	Blank
0	1	Dim
1	0	Half Brightness
1	1	Full Brightness

L1	L0	Linetype
0	0	Solid Line
0	1	Intensified End Point
1	0	Long Dashes
1	1	Short Dashes

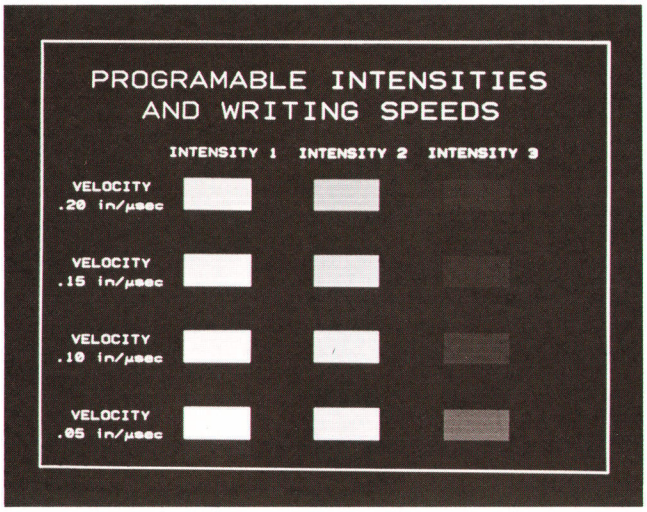


Fig. 5. *Twelve levels of brightness can be obtained by choosing combinations of one of the four writing rates and one of the three brightness levels.*

W1	W0	Writing Speed
0	0	0.20 inch per microsecond
0	1	0.15 inch per microsecond
1	0	0.10 inch per microsecond
1	1	0.05 inch per microsecond

The plot command will move the beam to a specific X-Y location with the beam either on or off. The command word contains either the X coordinate or the Y coordinate, so that two plot command words are sent to specify an X-Y location. The beam will move only after receiving the Y coordinate. The format of the command is as follows:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	XY	PC	D	D	D	D	D	D	D	D	D	D	D

XY

0 = X coordinate (0-2047) as specified by D0-D10
1 = Y coordinate (0-2047) as specified by D0-D10

PC (Beam control bit)

0 = Move (draw vector with beam off)
1 = Draw (draw vector with beam on)

The graph command can be used when the data points are always the same X increment apart. If the system sends the 1345A that X increment, the 1345A will store it and au-

	Commands	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1) SET:	Full Brightness Solid Line 0.05 in/μs	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0
2) PLOT:	X Position = 1024	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
3) PLOT:	Y Position = 1024 Beam is off; Move	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
4) GRAPH:	Delta-X = 512	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
5) GRAPH:	Y Position = 512 Beam is on; Draw	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
6) GRAPH:	Y Position = 1024 Beam is on; Draw	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
7) TEXT:	ASCII 65 = "A" Size = 1.5 × Rotation = 0 Degrees	0	1	0	0	1	0	0	1	0	1	0	0	0	0	0	1

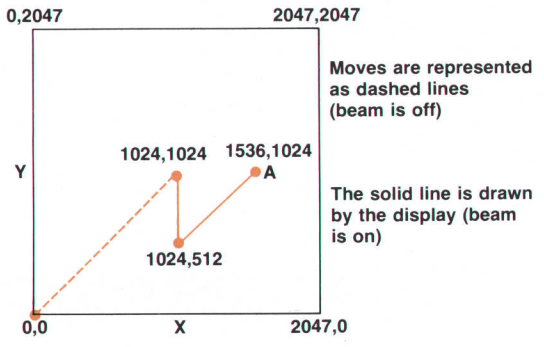


Fig. 6. *A sample 1345A command sequence and the resulting picture.*

tomatically increment the current X position by that X increment whenever GRAPH-Y data is sent. This means that after sending the X increment (delta-X), the system only needs to send GRAPH-Y values. This allows the system to use less memory to store a picture. The format of this command follows:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	XY	PC	D	D	D	D	D	D	D	D	D	D	D

XY

0 = Set delta-X increment (specified by D0-D10)
1 = Y coordinate (specified by D0-D10)

PC (Beam control bit)

0 = Move (draw vector with beam off)
1 = Draw (draw vector with beam on)

The text command will draw a specified character at the X-Y coordinate previously specified by a plot or graph command. The user may choose any combination of one of four character sizes and one of four rotations. The character is specified by the ASCII equivalent given in Table I. The text command format is:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	S1	S0	R1	R0	ES	A	A	A	A	A	A	A	A

ES

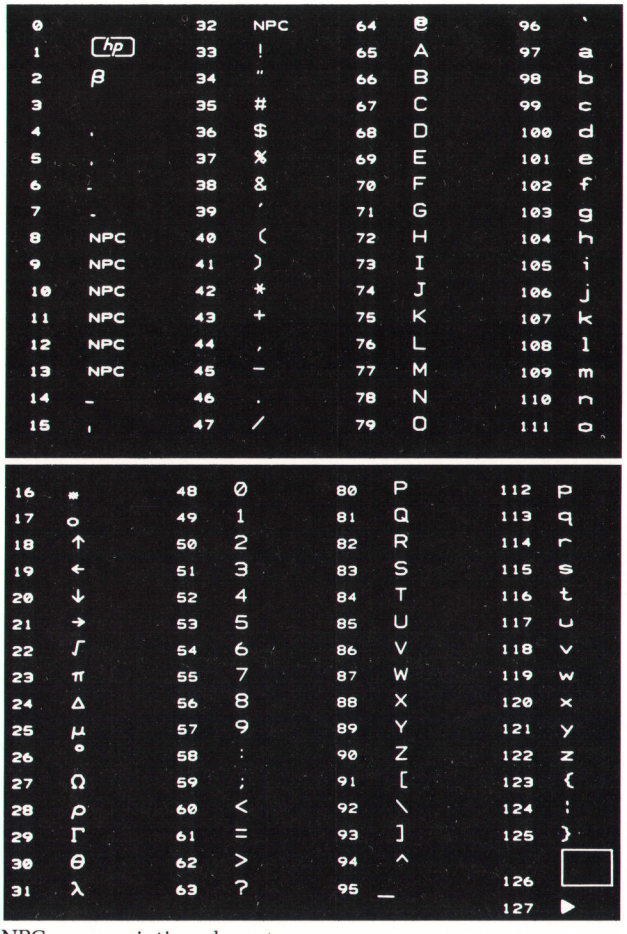
0 = Use previous size and rotation
1 = Establish new size and rotation using R1-R0 and S1-S0

R1	R0	
0	0	0 Degrees
0	1	90 Degrees
1	0	180 Degrees
1	1	270 Degrees

S1	S0	Size	Width × Height (in Addressable Points)
0	0	1 ×	24 × 36
0	1	1.5 ×	36 × 54
1	0	2.0 ×	48 × 72
1	1	2.5 ×	60 × 90

D7-D0 contain the ASCII code.

Table I
1345A Character Set



0	no operation	32	space	64	@	96	`
1	HP logo	33	!	65	A	97	a
2	beta	34	"	66	B	98	b
3	no operation	35	#	67	C	99	c
4	upper-half tic	36	$	68	D	100	d
5	lower-half tic	37	%	69	E	101	e
6	left-half tic	38	&	70	F	102	f
7	right-half tic	39	'	71	G	103	g
8	backspace	40	(	72	H	104	h
9	½ shift down	41	)	73	I	105	i
10	line feed	42	*	74	J	106	j
11	inv. line feed	43	+	75	K	107	k
12	½ shift up	44	,	76	L	108	l
13	carriage return	45	−	77	M	109	m
14	horizontal tic	46	.	78	N	110	n
15	vertical tic	47	/	79	O	111	o
16	centered *	48	0	80	P	112	p
17	centered °	49	1	81	Q	113	q
18	up arrow	50	2	82	R	114	r
19	left arrow	51	3	83	S	115	s
20	down arrow	52	4	84	T	116	t
21	right arrow	53	5	85	U	117	u
22	square root	54	6	86	V	118	v
23	pi	55	7	87	W	119	w
24	delta	56	8	88	X	120	x
25	mu	57	9	89	Y	121	y
26	° (degree)	58	:	90	Z	122	z
27	ohm	59	;	91	[	123	(
28	rho	60	<	92	\	124	|
29	gamma	61	=	93	]	125	)
30	theta	62	>	94	^	126	box
31	lambda	63	?	95	_	127	shaded triangle

NPC = nonprinting character

Instrumentation Graphics

The 1345A Digital Graphics Display is designed to meet the display requirements of electronic measurement instruments such as oscilloscopes, spectrum analyzers, network analyzers, curve tracers, and waveform analyzers.

The important aspects of any instrumentation graphics picture are resolution, brightness, the amount of data displayed, and the data update speed.

Addressable resolution is the incremental accuracy with which the electron beam can be positioned with the screen area. It is specified as the number of points along the horizontal axis and the number of points along the vertical axis. A high-resolution picture can present finer waveform details, such as noise spikes.

The ideal display should have enough brightness range to be useful in either a bright outdoor environment as in a portable instrument, or a darkened laboratory environment as in a bench-top instrument. It should show enough data and update it fast enough to keep up with transducer or measurement instruments' data acquisition and processing speeds.

Other essential characteristics of an instrumentation graphics display module are a high-quality picture, flexible packaging for easy mounting and minimum space requirements, and low power consumption to minimize the host instrument's cooling requirements and power supply load. The 1345A has these features, along with an ASCII character generator for labeling and identification of softkey functions, and the ability to generate different linetypes and different intensities to separate one waveform from another.

CRT Technology

There are two methods of deflecting the electron beam in a cathode ray tube (CRT): electromagnetic and electrostatic. Electromagnetic deflection uses magnetic fields to deflect the beam, while the electrostatic methods uses electric fields. It takes more energy and more time to change a magnetic field than an electric field. Therefore, the electrostatic deflection method can draw or update a picture much more quickly, and consumes less power. However, electrostatic CRTs are more expensive.

There are also two ways to scan the beam over the CRT screen. One method uses a fixed format, commonly known as raster-scan, and the other uses a random vector format and is called directed-beam. The raster-scan method scans the entire CRT screen one line at a time even when the beam is off or there is no data to present on the screen. This fixed-format scanning method makes the deflection circuit simple but limits addressable resolution, because the higher the resolution the longer it takes to scan the screen if the light output is to remain the same.

The directed-beam method moves the electron beam in a random vector format only where data needs to be presented on the CRT screen. Because the beam is moved from one point to the next in a straight line, line quality remains high compared to raster scan, in which a line appears as series of dots. Therefore, the directed-beam method has a higher data update speed, higher addressable resolution, and better straight-line quality.

Many computer data terminals today have CRT displays using electromagnetic deflection and the raster-scan format. The CRTs are current-driven through a yoke and a tuned circuit. The electromagnetic deflection and raster scan make an attractive combination for reasons of cost and simplicity.

The 1345A uses electrostatic deflection and the directed-beam format because it is intended as a low-power, high-resolution display module with real-time picture update speed to satisfy instrumentation graphics needs.

Fig. 6 shows a sample command sequence and the resulting picture.

Refreshing the Display

The system is required to resend all picture data to the 1345A at a minimum rate of 50 Hz. Below a 50-Hz refresh rate, the display may begin to flicker. Recommended refresh rate is approximately 60 Hz.

If the user does not wish to worry about refreshing the picture data, the 1345A can be ordered with an internal memory option. This option supplies a 4K×16-bit read/write memory. The 1345A will automatically refresh the display with the picture data contained in the memory. Since the system only has to write the picture data once with this option, it is often possible to specify a lower-performance microprocessor when designing the system.

The memory interface uses the same 16-bit data bus as the standard 1345A for both data and address information. The address used for a memory read or write cycle is stored in an address pointer on the memory board. The user may load this address pointer via the data bus and then proceed to write or read picture data. After each access of picture data, the address pointer is automatically incremented.

Four interface signals control operation of the memory board, as follows (X = don't care):

RD	WR	DS	AO	Memory Action
X	X	1	X	None
0	1	0	X	Read from memory
1	0	0	0	Write to address pointer
1	0	0	1	Write to memory

Memory Programming Example

Address	Contents
0000	Jump to 1002
0001 to 1000	Picture A
1001	Jump to 1002
1002 to 2002	Picture B
2003	Jump to 2062
2004 to 2060	Graticule A
2061	Jump to 2062
2062 to 2147	Graticule B
2148	Jump to 0
2149 to 2255	Set of Labels
2256	Jump to 0
2257	Memory

In this example:

- **Picture A is not displayed**
- **Picture B is displayed**
- **Graticule A is not displayed**
- **Graticule B is displayed**
- **The labels are not displayed**

Fig. 7. *The jump command in the refresh memory will cause the display to jump to any desired picture element. Animation and scrolling can be achieved using this command.*

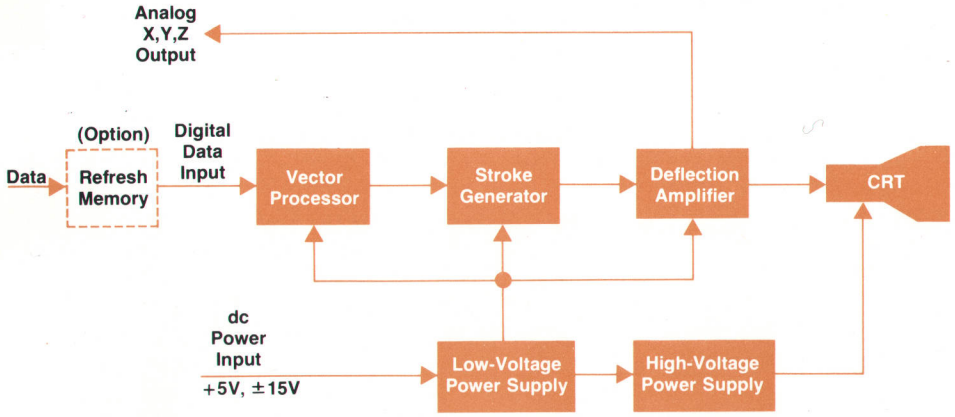


Fig. 8. *1345A block diagram.*

Two additional signals provide added flexibility. An acknowledge signal is output for every cycle. Since the memory has a constant access time of 320 ns, the use of this signal is optional. An input for external synchronization of the picture is also supplied. If not used, the picture is refreshed by an internal circuit at a rate of approximately 60 Hz.

Two types of data words can be written into the memory. The first is picture data, which uses the 1345A data format described earlier. The second allows the user to direct the refresh circuitry to jump around picture data. This jump command is written into the memory but is not sent to the display. Its format follows:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A

D0-D11 specify the next data word to be sent to the 1345A display.

The jump command allows the user to write graticules, labels, or other picture elements into memory upon power-up and display them only when needed. A jump command inserted into the memory will cause the display to jump to any desired picture element (see Fig. 7). The user may also use the jump command to create animation on the screen by successively jumping to a series of pictures. These prestored pictures can be any size, limited only by the memory size. Scrolling of data or text can also be achieved by using the jump command.

Line Generation

Fig. 8 is the block diagram of the 1345A Display. The stroke generator takes the digital X and Y data from the vector processor and generates voltages to drive the CRT via

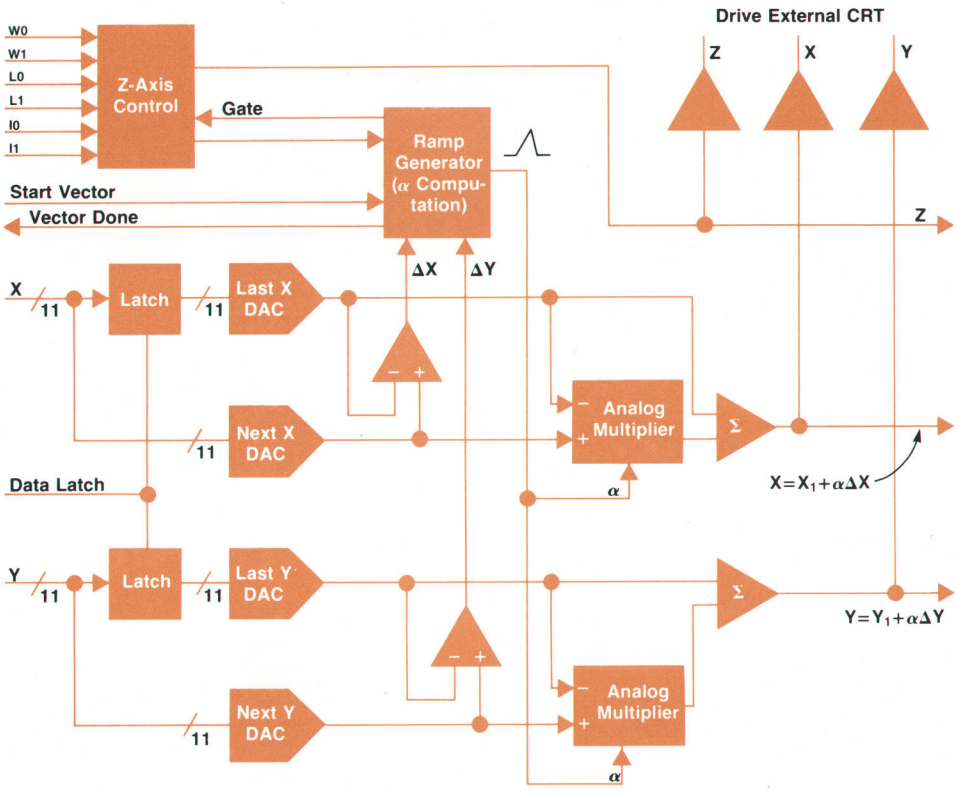


Fig. 9. *The stroke generator implements the linear parametric equations for a straight line.*

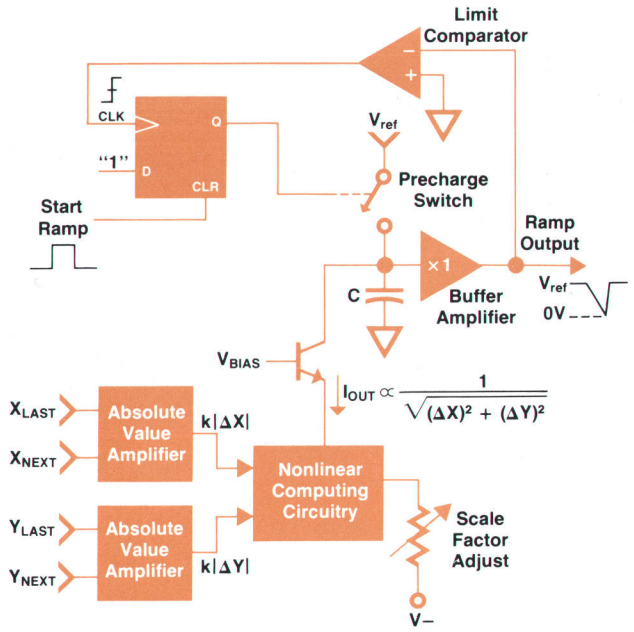


Fig. 10. *The ramp generator keeps the writing beam velocity constant regardless of the length of the line being drawn. Thus all lines have the same intensity unless different intensities have been programmed.*

the deflection amplifiers.

The linear parametric equation for a straight line with end points at (X_1, Y_1) and (X_2, Y_2) is:

$$X = X_1 + \alpha\Delta X \text{ where } \Delta X = (X_2 - X_1)$$
$$Y = Y_1 + \alpha\Delta Y \text{ where } \Delta Y = (Y_2 - Y_1)$$
$$0 \leq \alpha \leq 1$$

The stroke generator implements these equations as shown in Fig. 9.

Varying α from 0 to 1 will trace out the line. If the slope $d\alpha/dt$ is constant while the vector length (L) changes, the writing beam velocity is not constant. This results in nonuniform brightness of vectors—long vectors dim, short vectors bright. To achieve uniform brightness regardless of vector length, a scheme of intensity drive correction can be implemented.

However, a more elegant solution is to keep the beam velocity constant. To keep dL/dt constant, the slope $d\alpha/dt$ must vary inversely as $\sqrt{(\Delta X)^2 + (\Delta Y)^2}$.

The circuitry used to generate such a ramp function in the 1345A is diagrammed in Fig. 10.

Initially, the Q output of the flip-flop is high, and the precharge switch is closed, connecting the top of the capacitor to V_{ref}, and holding the ramp output at the reference voltage.

A negative-going ramp is generated when the flip-flop is cleared, opening the precharge switch and allowing the capacitor to be discharged linearly by the constant current output of the computing circuitry. Because the output current of the computing circuit is inversely proportional to the length of the line being traced, $\sqrt{(\Delta X)^2+(\Delta Y)^2}$, the slope of the ramp function is:

$$\frac{d\alpha}{dt} \propto \frac{dv}{dt} = -\frac{I_{out}}{C} \propto \frac{1}{\sqrt{(\Delta X)^2+(\Delta Y)^2}},$$

as required.

Finally, when the ramp output reaches zero volts, the limit comparator is tripped, clocking a one into the flip-flop and closing the precharge switch. The capacitor is quickly charged to the reference voltage, and the initial condition is restored.

Vector Processor

The vector processor accepts data from either a host processor or a refresh memory and performs the following functions:

- Monitor the set condition command and control the following:
  - gray scale (intensity)
  - linetypes
  - writing speeds
- Handshake with the stroke generator and pass a single PLOT-X/PLOT-Y 11-bit absolute data word
- Convert graph mode data to output absolute data values for the stroke generator.
- Convert text ASCII values to absolute stroke data.

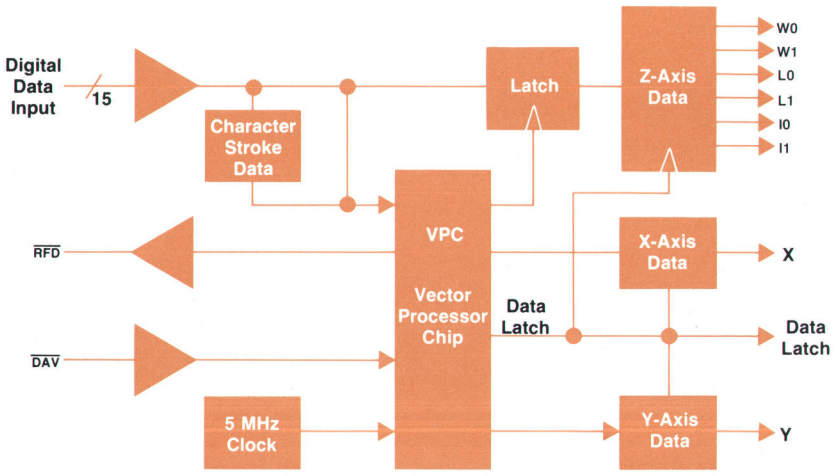


Fig. 11. *The vector processor accepts input data and processes it for the stroke generator. The VPC is a special NMOS/CMOS integrated circuit chip.*

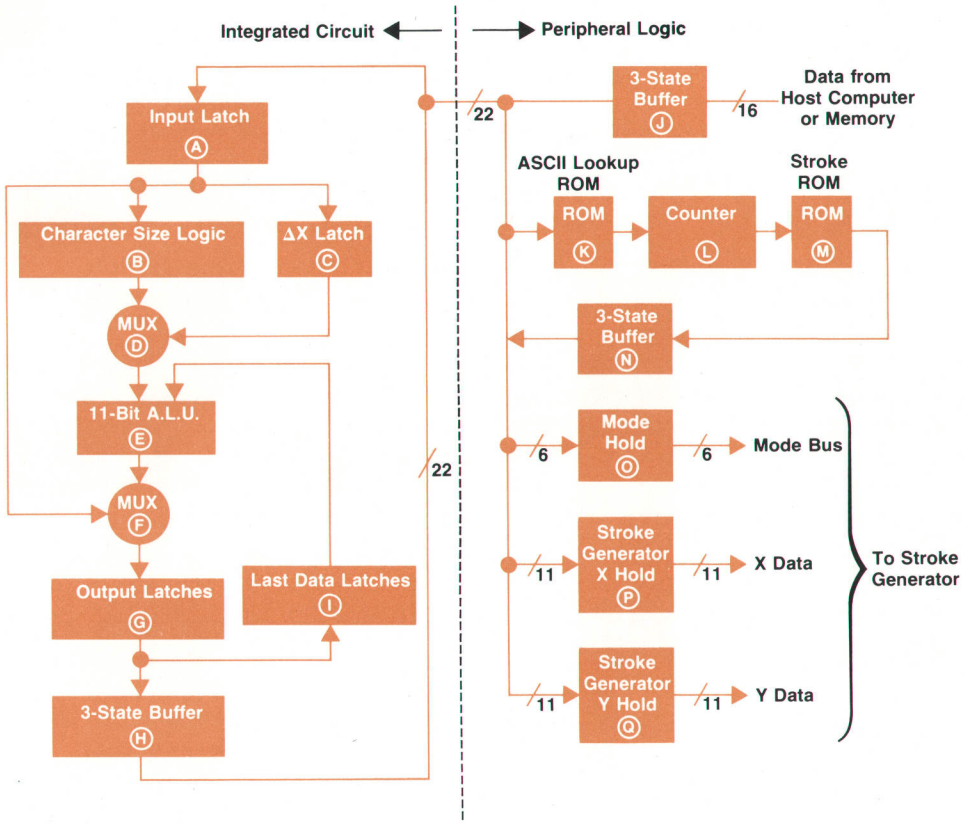
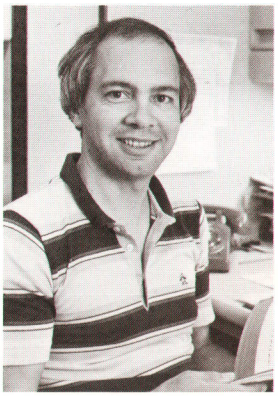


Fig. 12. *VPC architecture and operation.*

The major design constraints were a result of the space, power, and speed requirements. The board space available was less than 320 cm² and power dissipation had to be less than 5 watts. The speed required was dictated by the stroke generator, which can draw some vectors in as little as 1.5 μs. Thus the vector processor had to be designed to set up each vector in at most 1 μs.

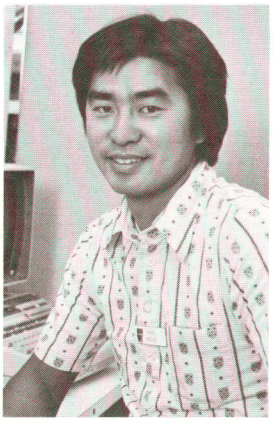
The space and power constraints indicated an integrated-circuit implementation. After due consideration, an NMOS/CMOS process was chosen and a special vector processor chip (VPC) was designed. Fig. 11 shows the block diagram of the vector processor based on the VPC.

An additional requirement for very smooth characters suggested a character made with strokes rather than a raster character approach. This, combined with the need for mul-



Thomas J. Zamborelli

Tom Zamborelli received his BSEE degree from Colorado State University in 1966 and joined HP the same year. He has contributed to the design of the 1801A, 1805A, and 1808A Vertical Amplifiers, served as project leader for the 1720A Vertical Amplifier and the 1340A Display, and designed portions of the 1345A Graphics Display. This is his second article for the HP Journal. Tom was born in Sopris, Colorado and now lives in Colorado Springs. He is married, has two sons, and spends much of his free time "hacking tennis balls."



Kunio Hasebe

Kunio Hasebe grew up in Kaneohe, Hawaii and attended the University of Hawaii, graduating with BSEE and MSEE degrees in 1971 and 1972. He joined HP's International Operations as a staff engineer in 1973 and four years later moved to the Colorado Springs Division, where he has served as a design engineer on the 1350A Graphics Translator and as project manager for the 1345A Graphics Display. This is his second appearance in the HP Journal. Kunio is married, has a son, lives in Colorado springs, and enjoys cross-country skiing and driving in the mountains of Colorado.

William R. Mason

Bill Mason has been with HP since 1968. He has contributed to the design of the 1332A, 1333A, 1335A, and 1336A Display Modules, the 1350A Graphics Translator, and the 1345A Graphics Display. A graduate of the University of Colorado, he received his BSEE degree in 1972. Bill is married, has two children, and enjoys golf, fishing, and skiing.

tiple character sizes and rotations and the 1345A graph mode, led to the architecture shown in Fig. 12 for the VPC.

The function of the VPC can be seen by looking at its operation in each of the four 1345A modes. Letters refer to blocks in Fig. 12.

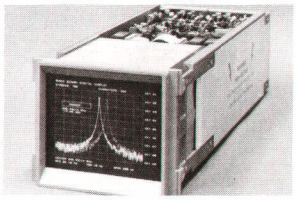
1. Set condition. Data is latched onto the VPC into A and sent to the stroke generator via latch O.
2. Plot absolute. Data is input via J to A, through F, G, and H, and output to P and Q for stroke generator use.
3. Graph absolute. The X data is first latched into C. Thereafter, only Y data is passed to A via J. Data is output to the stroke generator for X via C, D, E, F, G, H and P. For Y data the data path is A, F, G, H and Q.
4. Character data is handled somewhat differently. The ASCII data is latched into L via J and K. Thereafter, the character stroke data is read from the stroke ROM M via N into A until the last stroke is read. Character size and rotation is determined in B, D, and E. Data is then output through F as before in plot absolute form.

Acknowledgments

The authors wish to express a special thanks to three other 1345A design team members. These three people made their presence felt in this short time period. They also made significant contributions to this article. They are Gary Pumphrey, who designed the stroke generator, Rod Orgill, who with Bill Mason designed the vector processor chip, and Scott Neal, who designed the memory option.

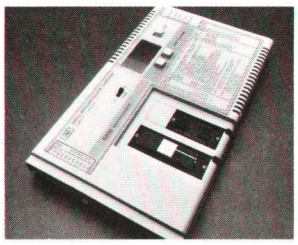
Thanks are also due Larry Brunetti and Walt Fisher for management support, Pete Berg for mechanical design, Wayne Helgoth and Bob Kenney for CRT design, Rich Davis for circuit design, Jack Benson, John Morgan, and Dave Bigelow of the Colorado Springs Division IC department, and George Latham and the Loveland Division IC department.

PRODUCT INFORMATION



HP Model 1345A Graphics Display Module

MANUFACTURING DIVISION:
Colorado Springs Division
1900 Garden of the Gods Road
Post Office Box 2197
Colorado Springs, Colorado 80901 U.S.A.
TECHNICAL DATA: HP Publication 5953-3967
PRICE IN U.S.A.: $3350. OEM prices available.



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